NOVEMBER 24, 1982

A CAHNERS PUBLICATION

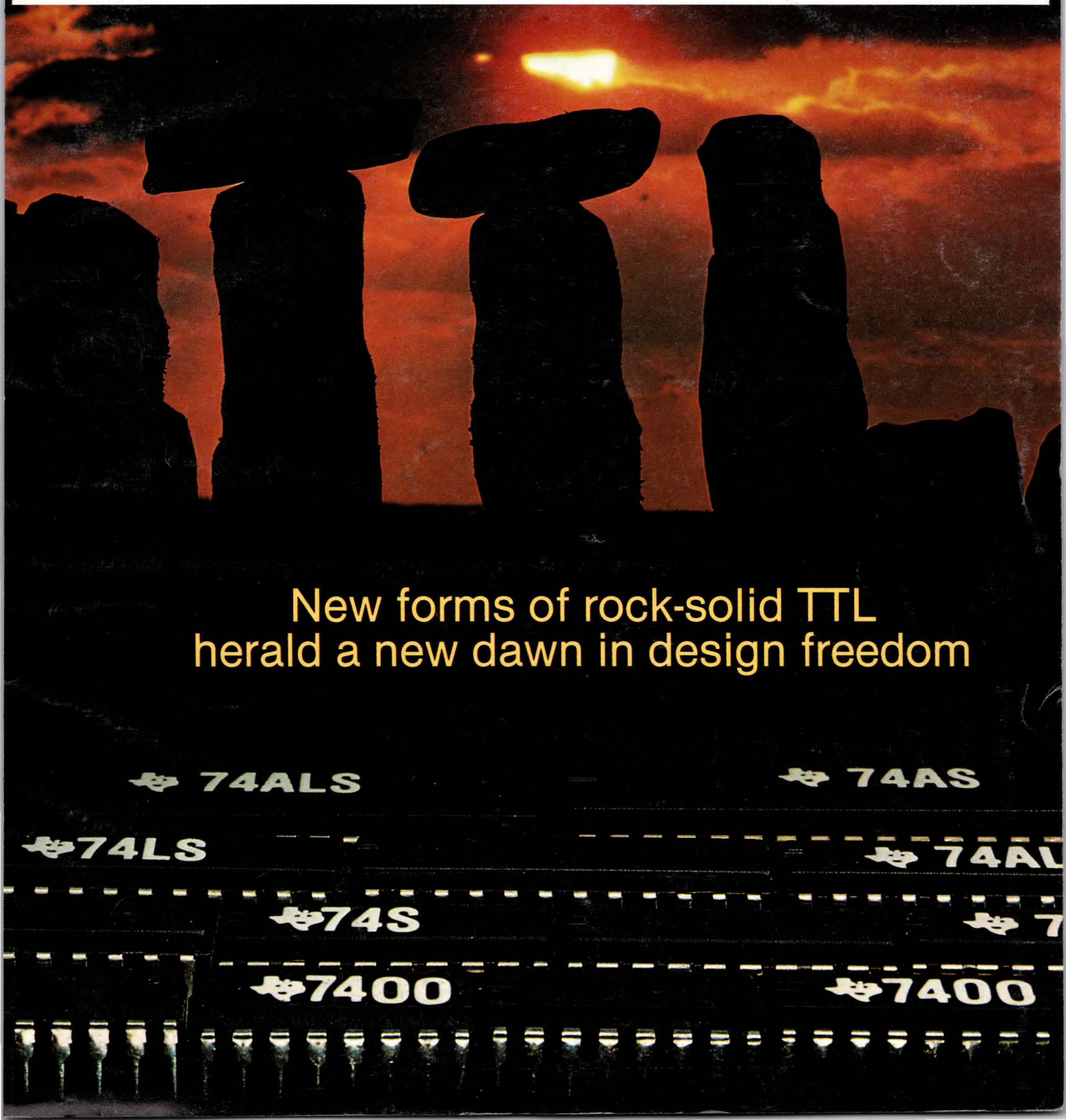
EDN

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

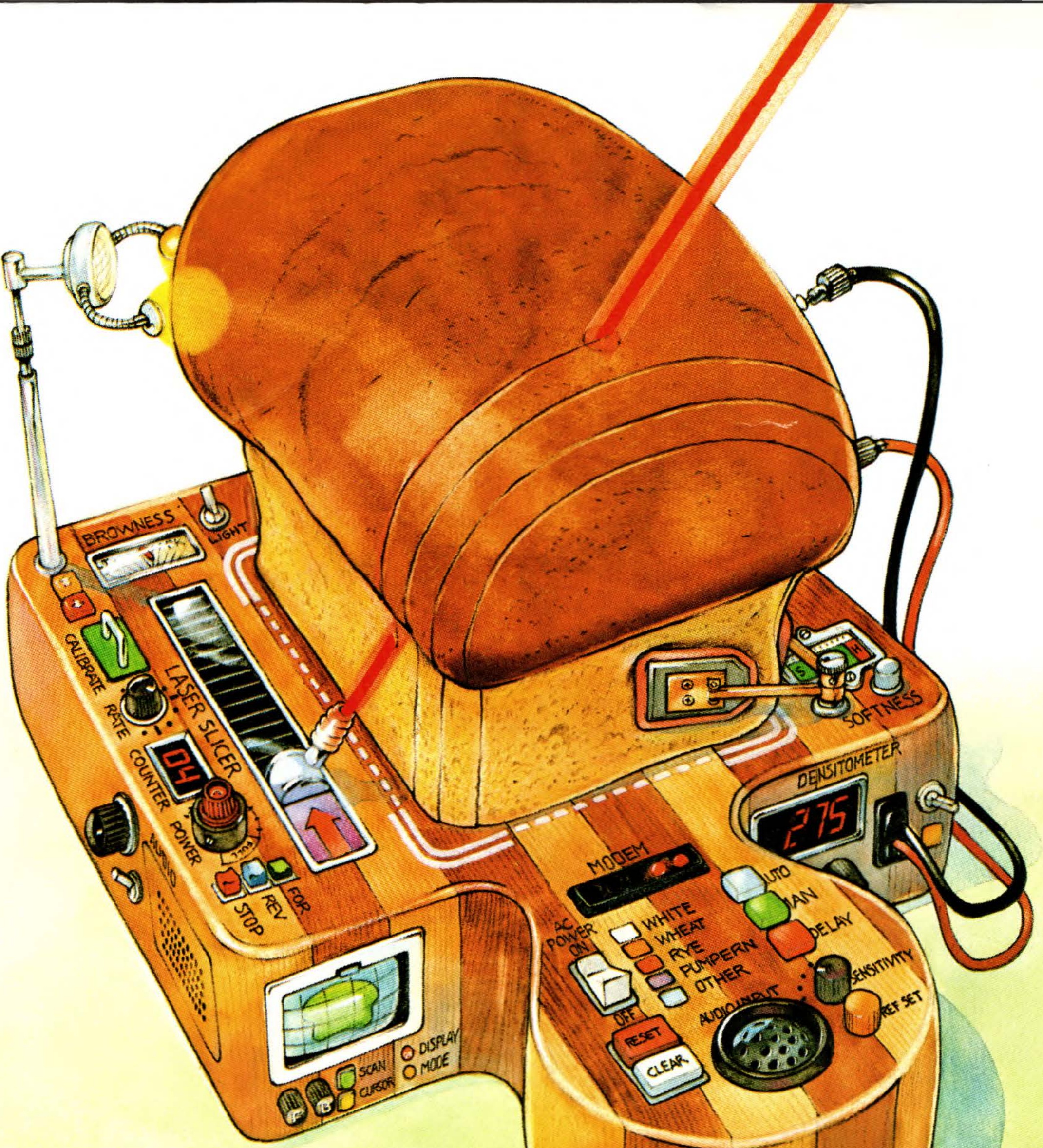
Optimize performance through proper op-amp choice

Hard-disk controller simplifies interfaces

Multibus analog I/O cards serve diverse needs



New forms of rock-solid TTL herald a new dawn in design freedom



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For Resistor Network Brochure circle 1

For Resistor Selection Guide circle 98

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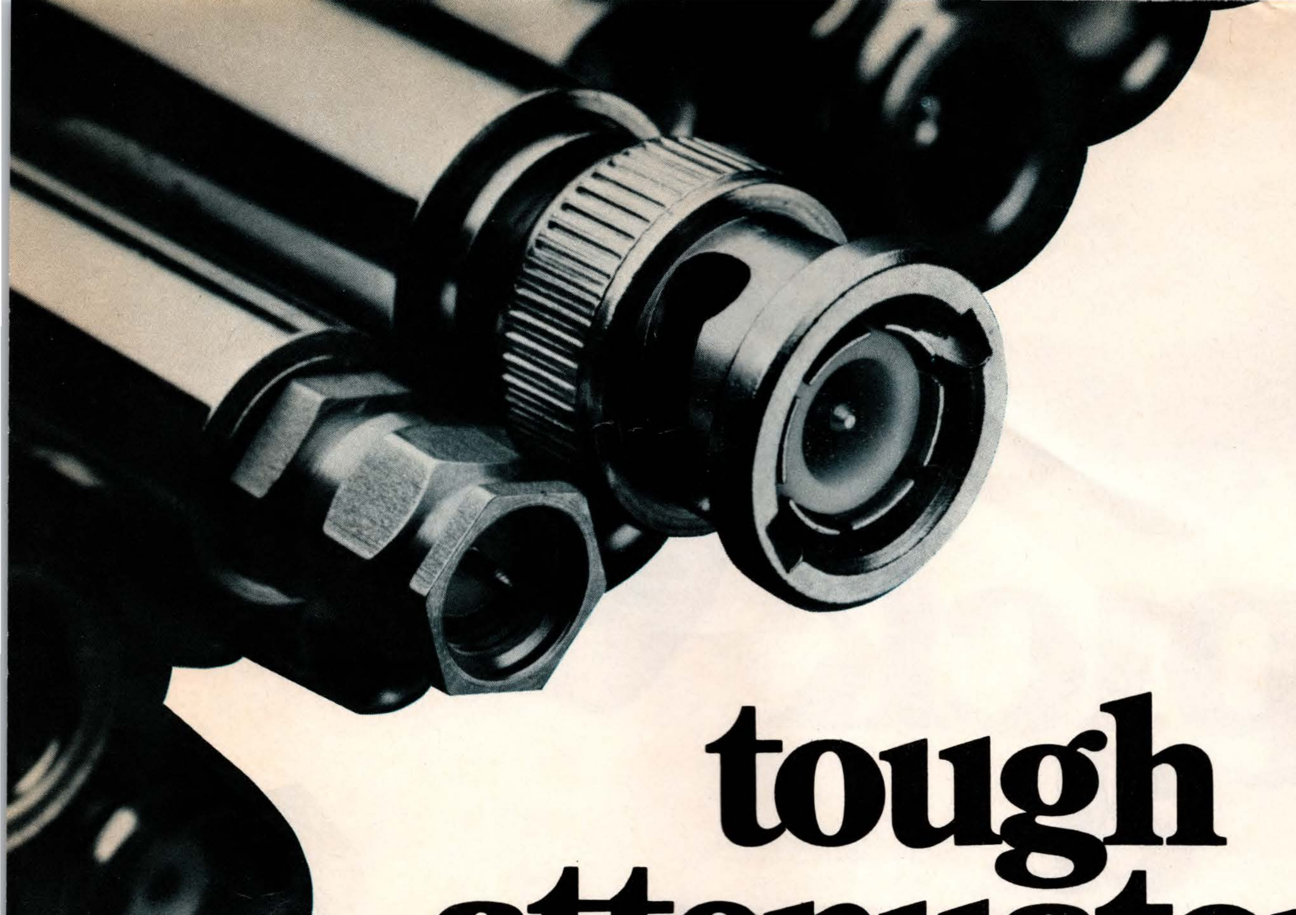

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Model	Attenuation, dB	Attenuation Tolerance	Frequency MHz	Attenuation Change over Frequency Range, MHz DC-1000	Attenuation Change over Frequency Range, MHz 1000-1500	VSWR Max. (50 ohms) DC-1000	VSWR Max. (50 ohms) 1000-1500
—AT—3	3	±0.2dB	DC-1500	0.6dB	1.0dB	1.3:1	1.5:1
—AT—6	6	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1
—AT—10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1
—AT—20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1

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*Units are not QPL listed

MODEL	SRA-1	TFM-2	SBL-1	SBL-1X	ASK-1
FREQUENCY, MHz					
LO, RF	.5-500	1-1000	1-500	10-1000	1-600
IF	DC-500	DC-1000	DC-500	.5-500	DC-600
CONVERSION LOSS, dB					
one octave bandedge	6.5	6.0	7.5	7.5	7.0
total range	8.5	7.0	8.5	9.0	8.5
ISOLATION, dB, L TO R					
lower bandedge	50	50	45	45	50
mid range	40	40	35	30	35
upper bandedge	30	30	25	20	20

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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EDN

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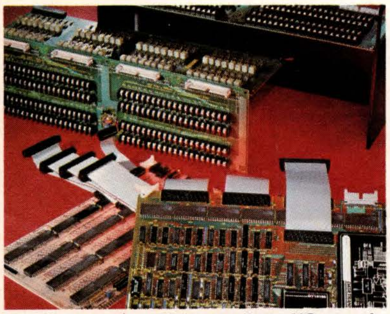
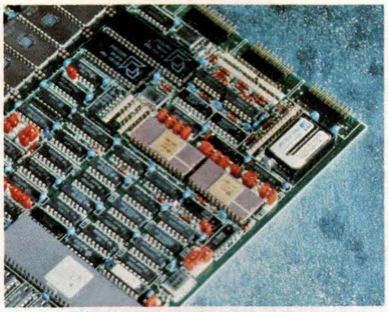
DESIGN FEATURES

TECHNOLOGY UPDATE

Contents continued on pg 7



Multibus-compatible analog I/O cards *simplify a variety of analog-system design tasks and span a wide range of performance capabilities (pg 45).*



Double-Eurocard 16/32-bit µC modules *accommodate high-performance industrial applications, providing multimaster compatibility with 8/16-bit boards (pg 264).*

On the cover: *Advances in rock-solid TTL promise to keep this familiar design aid viable in many applications (pg 94). (Photo courtesy Texas Instruments Inc)*

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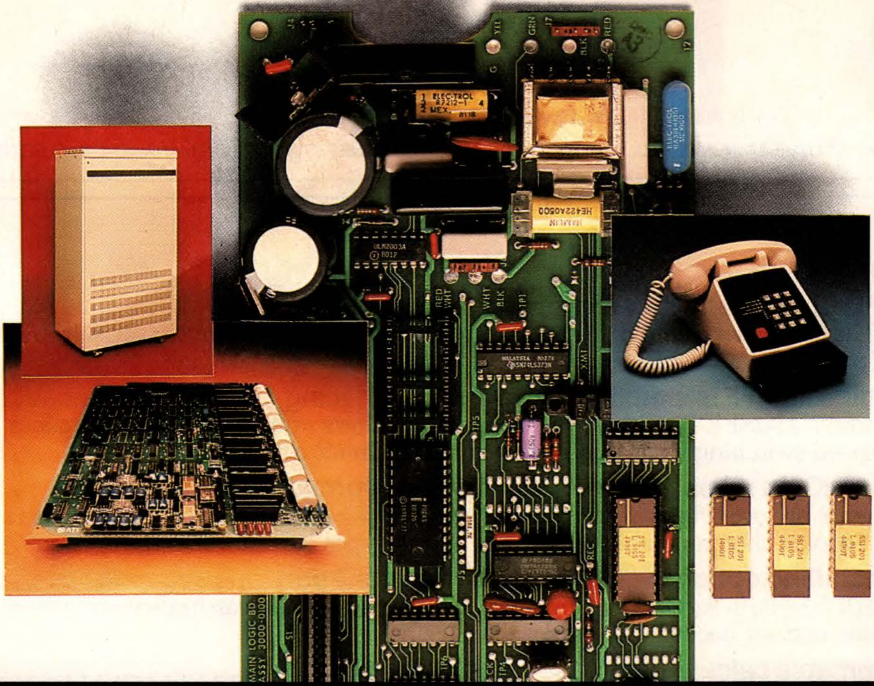

PCB's and photos of PBX and transaction terminal courtesy of American Telecom, Inc. and DMC Systems, Inc.

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CIRCLE NO 4

EDN NOVEMBER 24, 1982

Continued from pg 5

TECHNOLOGY UPDATE: NEW PRODUCTS

DESIGN IDEAS

µC DESIGN TECHNIQUES

NEW PRODUCTS

A QUESTION OF LAW

LOOKING AHEAD

DEPARTMENTS

The Part

Most second-source agreements go something like this: "Here's the mask, you figure it out."

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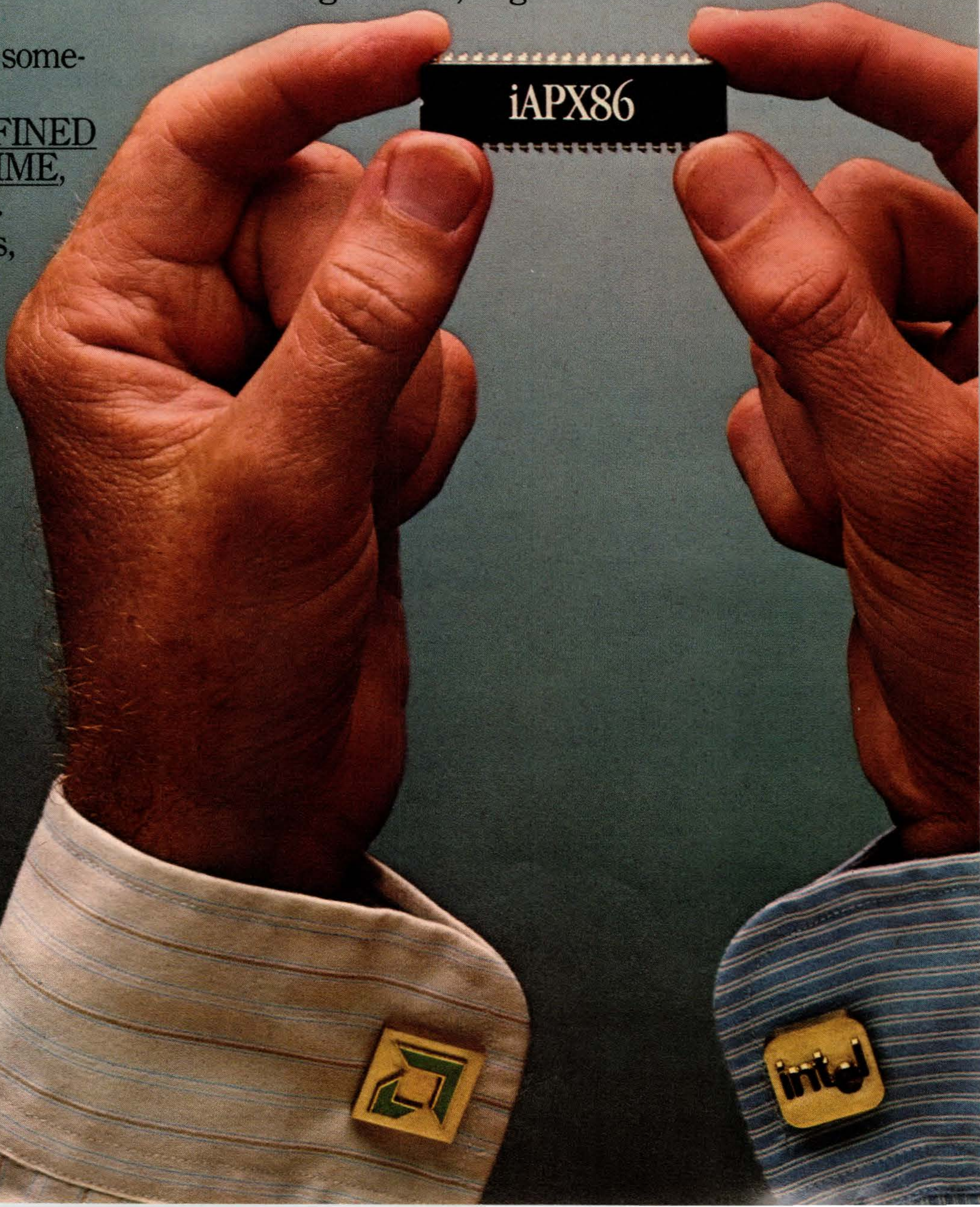


HARRIS SPE

GETTING THE FACTS ON PROGRAMMABLE MICROPOWER OP AMPS

Holmes walked into the newspaper office and lectured the startled young reporter for his misinterpretation of the facts on PMI's OP-22 programmable micropower op amp.

It was at an SIA dinner meeting that Sherlock Holmes encountered Billy Durham, local reporter for *Electronics Gazette*. Holmes sat in quiet bemusement as the brash young man held court over a Marriott table of eight, not realizing that the attention being paid to him reflected less on his charm than on the power of his publication.

"I'm into an investigative piece on micropower op amps," Durham was saying. "One of my sources who designs portable instrumentation says the linear circuit houses have really overlooked it. Nothing out there works well at low power with the kind of gain you need for battery-powered instruments like handheld voltmeters and portable data acquisition systems."

Billy's audience for the most part only feigned interest, having just sat down from a rigorous cocktail hour, but a few felt compelled to respond.

"I guess the only answer is the LM4250C," one said. "That's currently the industry standard. At least it's cheap, fast, and has a programmable supply current."

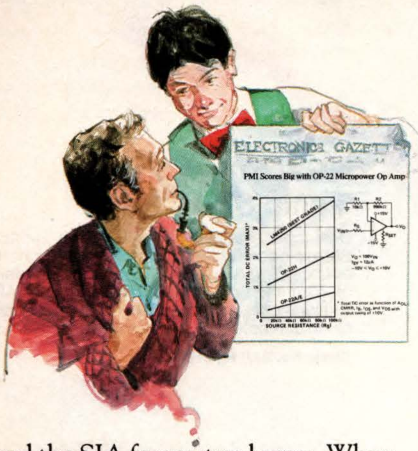
Suddenly Holmes could hold his silence no longer. "Ah, my friends, but what tradeoffs Billy's source would have to make in performance, whether he uses the LM4250, MC1776, or any of the others of that genre. They are all low in price, but they are also low in performance, particularly when it comes to gain, input offset voltage, **CMRR and PSRR.**"

"Then what's the answer, Mr. Holmes?", the intrepid reporter queried.

"I'm no expert, of course," Holmes said, "but I've heard that PMI's new OP-22 programmable micropower op amp is the first to offer the performance specifications of precision op amps like the OP-07 or OP-12 for low-frequency, high-gain applications. As an objective reporter, you should certainly look at this PMI OP-22 data sheet."

As the detective handed it across the table, the house lights dimmed

A contrite Billy Durham showed Holmes his follow-up story on industry acceptance of the OP-22, highlighted by a Page 1 graph tracking dc error vs. source resistance.



and the SIA forecasters began. When Holmes looked again, the young reporter had vanished.

A week later, Holmes sat reading Billy Durham's by-lined report in *Electronics Gazette*.

"I don't believe it, Watson," he cried out.

"How's that, Holmes?" Watson said, looking up from the Rubik's Cube™ that had absorbed him for weeks.

"That reporter we met at the SIA dinner. He garbled the facts by suggesting that 'a usually reliable industry source,' meaning me, I assume, 'said that to achieve precision performance in high-gain instrumentation operating from battery or solar-cell power sources, designers will have to scrap existing designs built around the standard LM4250 or comparable circuits in order to get the precision performance of PMI's new OP-22.' "

"Hmmm," Watson muttered. "Isn't that what you said?"

"Absolutely not," Holmes insisted. "The OP-22 is fully pin-compatible with the 4250, even though it offers an order of magnitude improvement in performance. At least he appears to have the specs right: Programmable supply current, 1μA to 400μA; single or dual supply operation; input offset voltage, 100 μV, with drift specified at 0.75μV/°C; high CMRR and PSRR of 115dB. And, of great significance—high open-loop gain of 1.8 million."

"Smashing," said Watson.

"Smashing indeed," Holmes replied. "In fact, those are the specs of which legends are made. But young Billy has misled the industry, I'm afraid."

An hour later, Holmes walked into the editorial offices of the *Gazette* and threw the paper on the desk of a very startled Billy Durham, who asked,

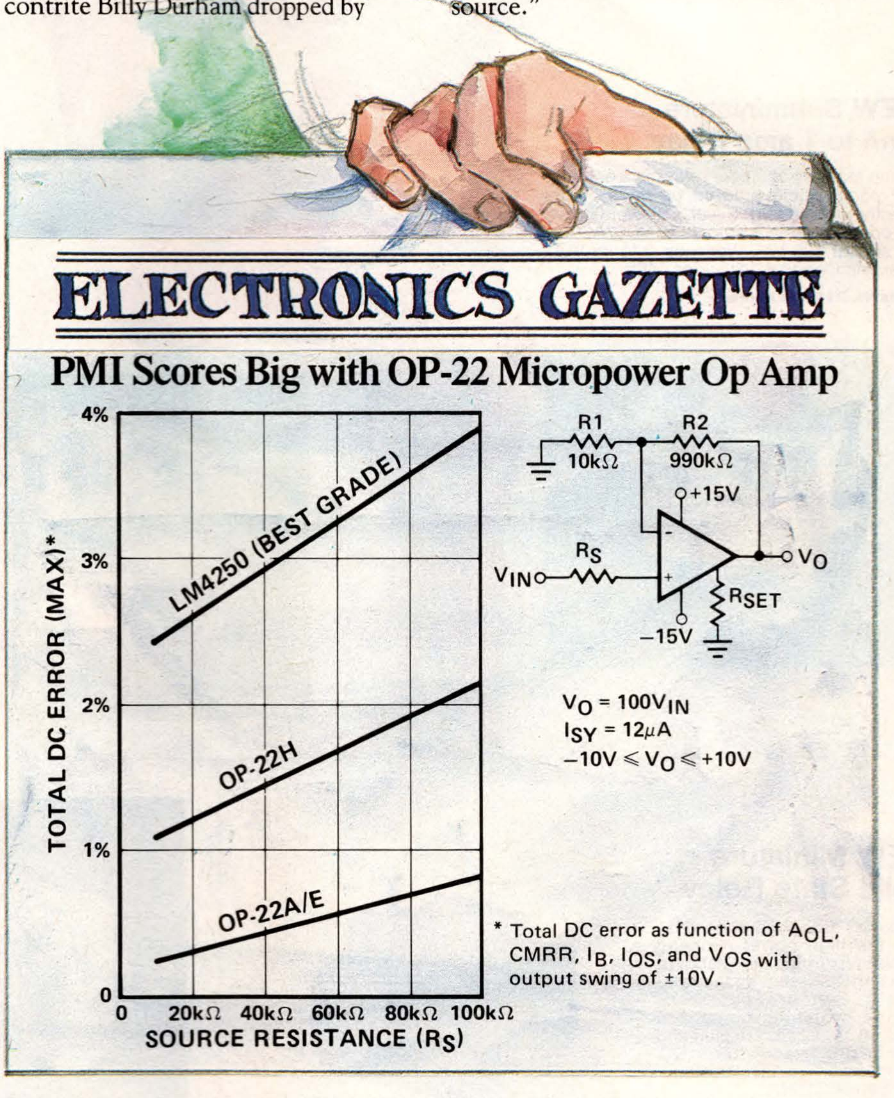
"Like my report, Mr. Holmes?"

"Your facts are straight, Billy, but your interpretation is wrong. Of course, the OP-22 is ideal for *new* designs. But its value is enhanced by the fact that it is pin-compatible with the 4250. In fact, I would hazard a guess that in any application where performance is more important than price, there isn't a 4250 socket around that couldn't be upgraded and made more *robust* with the OP-22. You owe it to your readers to tell them *all* the news that's fit to print, Billy."

It was a full two weeks later that a contrite Billy Durham dropped by Holmes' office at 221B Bayshore. "I wanted you to be the first to see my follow-up report on the OP-22," he said, proudly displaying the *Gazette's* story on the rapid industry acceptance of the OP-22's versatility and precision performance, highlighted by a graph tracking total dc error vs. source resistance.

"Well done," Holmes said. "You're an honor to your profession, Billy."

"Thanks, Mr. Holmes. And I appreciate your help so much that you'll notice this week I promoted you from *usually* reliable source to *highly* reliable source."



(TO SEE ALL THE EVIDENCE SHERLOCK HOLMES HAS GATHERED ON PMI'S NEW OP-22 PROGRAMMABLE MICROPOWER OP AMP, JUST CIRCLE THE READER SERVICE NUMBER OR CALL YOUR PMI REPRESENTATIVE.)

PMI

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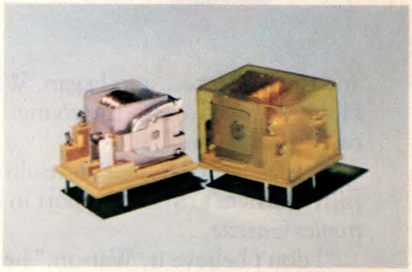

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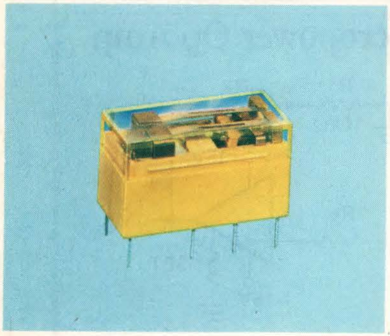

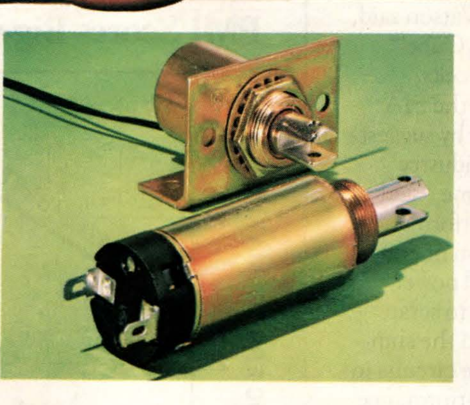

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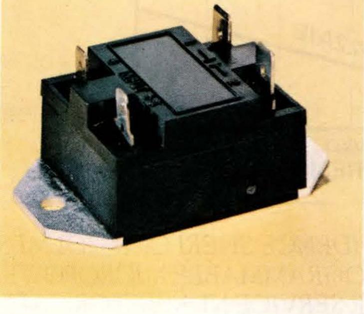

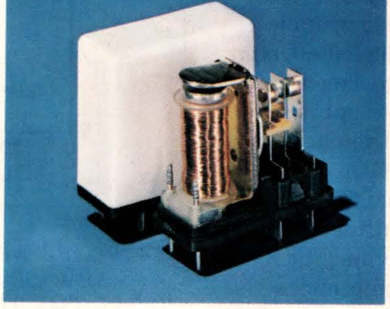

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Edited by Joan Morrow

News Breaks

DISK-CONTROLLER CARDS USE CUSTOM LSI TO IMPROVE PERFORMANCE

Introduced last week, SA1600 Series disk controllers from Shugart Associates (Sunnyvale, CA) provide complete device independence (you can use them with a variety of drives), while providing greater reliability and a lower cost than SA1400 Series controllers. On-board custom LSI circuitry accepts six generic commands from the host CPU—the controller takes care of all disk-specific control functions.—Ed Teja

COMPUTER CENTER SERVES AS TECHNOLOGY SHOWCASE

In addition to providing entertainment and information to Walt Disney's $1B Epcot Center in Lake Buena Vista, FL, the newly dedicated Sperry Univac computer central—a 40,000-ft^2, 2-level building—houses a real-time data-processing operation. As an equipment showcase, its computer systems educate, entertain and dramatize the fact that computers perform as helpful and essential tools for managing the world's workloads.

On site, four V77 minicomputers and related peripherals monitor the environment and control of special-effects events—such as those involving Disney's lifelike audio-animatronic robots—live shows and multiaudio-visual theater presentations at the center's Future World and World Showcase pavilions. Other computer-controlled facilities include a V77-800 minicomputer that directs the show monitor and control system; a V77-500 minicomputer that assists in tracking 4000 power, environment and security sensors; and two V77-800 systems that support the special-events control system.—George Kotelly

A PREVIEW OF COMDEX DEBUTS

You'll see some exciting new-product introductions if you go to Comdex in Las Vegas, NV next week (November 29 to December 2). For example, Micro Five (Irvine, CA) will show its 16-bit Series 1000 professional personal computer; Compupro (Oakland, CA) will unveil a family of small business systems based on its 8085/8088 CPU card; Media Systems Technology Inc (Irvine, CA) will demonstrate an automatic desktop copier for 96-tpi, 5¼-in. floppy disks; and International Anasazi Inc (Phoenix, AZ) will present an enhanced version of the Emulog 200 terminal that features a 7×9-character matrix and a detached keyboard.

In addition, Vertex Peripherals (San Jose, CA) will show its 5¼-in. Winchester drive, which uses a voice-coil actuator to achieve average access time of 30 msec—about one-third the time of standard 5¼-in. Winchesters. It's available in 30M-, 52M- and 72M-byte versions.

Finally, Archive Corp (Costa Mesa, CA) will display its newest streaming-tape drive—one that's form-factor compatible with 5¼-in. Winchester drives. You'll be able to choose models that furnish 20M or 45M bytes of backup. Prices will range from $850 to $1000 (OEM qty); deliveries should begin early next year.—Ed Teja

SINGLE-CHIP 4½-DIGIT A/D CONVERTER USES FEW EXTERNAL COMPONENTS

A potential de-facto standard for 4½-digit multimeter chips (much like its 7116 cousin is in 3½-digit applications), the ICL7129 from Intersil (Cupertino, CA) directly drives multiplexed LCDs with only a few external passive components. Accuracy is better than 0.005% FS, and resolution equals 10 μV. The CMOS design draws only 1 mA from a 9V battery and features low-battery detection and indication. In 40-pin plastic, ceramic or Cerdip, the device costs $19.95 (100).—William Twaddell

DEC-COMPATIBLE MASS-STORAGE UNIT HOLDS μC CARDS

Combining Winchester- and floppy-disk drives in a package with a Q-bus-compatible 8-slot card cage, Model RLX-10/01B from Charles River Data Systems (Natick, MA) sells for approximately $7100 (10). Its 10M-byte 5¼-in. Winchester is RL02 compatible, the 1M-byte 8-in. half-height floppy is RX02 compatible. The 7-in.-high unit's card cage accepts LSI-11/23 boards and provides 22-bit addressing.—Paul G Schreier

PLUG-IN SPEEDS UP COMPUTER-GRAPHICS SYSTEM

If the Tektronix 4051 graphics-computing system isn't fast enough for your application, try the 4051 advanced display pack from Periphicon (Beaverton, OR). This $1200 unit plugs into any 4051 ROM slot or expander to furnish a 15- to 150-fold speed increase, adding such capabilities as refreshed images and an interactive joystick. The plug-in produces complete graphic transformations and graphic primitive generators via a single call. Data format is eight times more dense than standard 4051 format allows.—Ed Teja

FAMILY OF SOFTWARE PACKAGES EASES CHIP DESIGN AND LAYOUT

VLSI Technology (San Jose, CA) has announced a set of integrated software tools to automate the design of ICs. Included are VIP, the firm's implementation program—an extension of MAINSAIL, a cell-compiler library that allows you to modify the size and structure of cells as required; STICKS, a graphics editor and design-rule checker that eases circuit layout; EXTRACT, which takes a layout and generates a net list in standard format; and VSIM, a logic simulator. This software runs on VAX-class hosts for multiuser setups and on the Apollo microcomputer for stand-alone workstations.—Paul G Schreier

FIRMS EXCHANGE CMOS, NETWORK TECHNOLOGY

Intel Corp (Santa Clara, CA), N V Philips (the Netherlands) and Signetics Corp (Sunnyvale, CA) have signed a 7-yr technology-exchange agreement that makes Philips/Signetics an alternate source for the 80C48, 80C49, 80C50 and 80C51 microcontrollers in Intel's CHMOS process. Intel, in turn, picks up the licensing and technology for Philips's I^2C and D^2B consumer/industrial serial data buses. Intel will also become an alternate source for Philips's MAB 8400 µC family—parts that mix the 8021's architecture with the 8048's instruction set. The companies will produce other devices, the first in the MAB8400 family.—William Twaddell

SPEAKING OF VOICE I/O...

A plug-in voice-input module for Apple II computers from Voice Machine Communications Inc (Villa Park, CA), Model VMC 2020C works in two ways: It comes with eight complete recognition vocabularies that suit use with popular word-processing packages, BASIC programming and other applications, or you can program your own vocabularies. The board comes with comprehensive software support on floppy disk and features 8k of on-card RAM for resident vocabularies of about 80 words. A fast upload routine lets you swap vocabularies quickly. The hardware and software costs $595; $450 in OEM (25) quantities.—Ed Teja

LOW-COST MODEM ACHIEVES FULL BELL 212A COMPATIBILITY

The Series 828 modem card from CTS Corp (Lafayette, IN) provides full compatibility with Bell 212A modem specifications, yet requires only 30 to 40 $in.^2$ of board space. Priced at $250 (OEM qty), it uses dual processors to furnish originate and autoanswer operation at 1200 and 300 baud. A $495 stand-alone version comes in a 5×8-in. box.—Ed Teja

SUBMIT YOUR PAPERS TO THE CUSTOM-IC CONFERENCE

The 1983 Custom Integrated Circuits Conference, scheduled for May 23 to 25 in Rochester, NY, will review papers on CAD; gate arrays, semicustom and full-custom ICs; custom analog ICs; applications; fabrication technologies; and interfaces and packaging. Submit 35 copies of a 250-word abstract of an original, unpublished work by January 31 to Dr Aris Silzars, Tektronix Inc, MS-50-479, Solid-State Group, Box 500, Beaverton, OR 97077.—Joan Morrow

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- **Choice of Single or Multiple Message Lines:** Each display location can handle up to 48 lines of information.
- **Minimum Wiring:** Displays are interconnected on a single RS422 cable loop.

Cherry Display Systems feature uniform color and high brightness, wide viewing angle and readability. They are available in a choice of 16, 20 or 24 characters per line.

Ready to install, these microprocessor-controlled systems include drivers, character generators, refresh memory and other electronics to provide many standard features—three end of line modes, horizontal scroll and more. Five levels of brightness are programmed to provide over 6 to 1 range of light output in 4 db steps.

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CIRCLE NO 7

OPTICAL LANs HOOK UP 240, 4096 TERMINALS

Facom 2880 Series optical-highway system from Fujitsu Ltd connects office-automation equipment such as computers, printers and facsimile machines via fiber-optic cables. The 2881 for small-scale local-area-network systems features 4M-bps transmission speed and can accommodate as many as 32 multiplexer nodes. This 120-circuit system, with maximum cable length of 96 km, hooks up as many as 240 terminals.

The 2883, for large-scale systems, provides 33M-bps transmission speed and connects as many as 64 nodes and a maximum of 4096 terminals through 2400 circuits. Maximum cable length equals 576 km. The 2881, with two 4-circuit nodes and one 32-circuit node, costs 3,600,000 yen ($13,585). The 2883, with eight 8-circuit nodes and one 64-circuit node, sells for $94,000.

Optional equipment for the optical-highway system includes two optical wireless modems that use light to transmit signals between terminals or the host computer and terminals. A low-speed modem costs $2264; the high-speed version, $3000.—Joan Morrow

1M-BYTE SEMICONDUCTOR MEMORY SEEN BY END OF '83

Toshiba Corp has joined the Nippon Telegraph and Telephone Corp "NTT-family" project formed for research and development on VLSI devices. Previously, Nippon Electric, Fujitsu Ltd and Hitachi Ltd—the prime suppliers of NTT's communication equipment—had exclusively worked on R&D projects for LSI products. The NTT project, which began in the fall of 1981, covers the development of 1M-byte semiconductor memory by the end of next year. Toshiba was allowed to join this R&D group because of its performance in a separate VLSI project and could become one of the VLSI suppliers to NTT after the device has been completed.—Joan Morrow

RED LED ACHIEVES 1000-mCD BRIGHTNESS

The brightest red LED available, according to manufacturer Matsushita Electron Industry, produces 1000-mcd brightness. It suits new application areas such as large-area dislays, panel illumination and optical communication within 100m. The firm has enhanced the device's brightness via a double-heterodyne-structure process used to manufacture laser diodes. It will begin production in January at a sample price of 300 yen ($1.13).
—Joan Morrow

5¼-IN. FLOPPY-DISK DRIVE MEASURES 120 × 350 × 165 mm

With the introduction of the TF-20 5¼-in. double-sided, double-density drive system, Epson has entered the Japanese floppy-disk market. Priced at 142,000 yen ($567), this Shugart SA400-compatible unit measures 120 × 350 × 165 mm and incorporates two slimline drives. Epson will initially sell the floppies only in Japan but expects to ship them overseas later.
—Joan Morrow

488-COMPATIBLE AUTOMATIC RF TEST SYSTEM HANDLES PASSIVE DEVICES

Using instruments from Rohde & Schwarz's (Munich, West Germany) IEEE-488-compatible line, the ZPV RF automatic network analyzer tests passive components. It consists of the ZPV vector analyzer, SMPC synthesizer, PUC bus controller, a printer and software, plus a variety of tests including reliable measurement of Q and capacitance of chip capactiors at frequencies higher than 800 MHz. At several hundred megahertz, Q factors to 13×10^{-4} can be measured with 15% uncertainty. The system permits measurement of resonant frequency, inductance and A_2 factor of coils at high frequencies.—Barrie Nicholson

VS

General Specifications

- USER SELECTABLE, WIDE INPUT RANGES OF 70-140VAC/140-280VAC (200-400VDC) VIA CONVENIENT DECISION JUMPER PLUG FURNISHED
- LINEAR TEMPERATURE CONTROLLER LIMITS CHASSIS TEMPERATURE TO SAFE LEVEL.
- DESIGNED TO MEET RIGOROUS SAFETY/ EMI REQUIREMENTS OF UL478, CSA C22.2, FCC DOCKET 20780, VDE 0730 PAR. 2P, AND VDE 0871.

The VS Series is a highly efficient, compact, triple output, off-line switching power supply. An advanced forward conversion technique used in the VS Series results in a lower component count and less self-heating than equivalent conventional designs, while maintaining a minimum full load efficiency of 75% over the 2:1 input ranges. Effective thermal management combined with 2-plane "L" bracket construction make the VS Series an extremely reliable, versatile power source.

FEATURES

EMI Agency Compliance All VS Series models are designed to meet the rigorous safety/EMI standards of UL478, VDE 0730 Par. 2P, CSA, C22.2, FCC Docket 20780, and VDE 0871.

Input Characteristics

The VS Series provides regulated output voltages even under deepest brownout conditions. Input over/undervoltage protection circuitry automatically shuts down the power source when predetermined min-max levels are exceeded. This circuitry protects the supply from damage when continuous input conditions as high as 150/300Vac are present on the 115/230Vac ranges, respectively. A negative true power fail signal with a holdup time sufficient to permit orderly system power down is produced when the input falls below 90-180Vac. In addition, a soft start circuit limits peak in-rush current to 15 Amps, even for on-off cycling. These features, in combination with two-line input fusing provides an input protection package unparalleled in the industry.

Output Characteristics

The VS Series incorporates a unique, automatically resettable, over-temperature control system which limits the maximum average chassis temperature to 105°C over all specified line, load, and ambient temperature conditions. Temperature sensing and control circuitry linearly foldback the output power automatically so that all heat sensitive components will not be stressed beyond their safe operating limits. Unlike most other designs, all major heat generating sensitive components are sufficiently heat sunk internally to attain full load operation to 71°C. The outputs are also overcurrent protected, via the automatically resettable power foldback circuit which is set for 160W. Additionally, the main output contains a continuously self-resetting overvoltage crowbar circuit which prevents load damaging transients. Each output can also withstand a reverse voltage up to its full rated output current.

Versatility

All outputs have isolated returns (up to 300 Vdc between outputs and chassis ground) for referencing to independent ground systems and for connecting outputs in various series combinations. Parallel operation of up to 3 units (main output) is possible. Isolated remote shutdown via TTL signals, remote sensing, and trim adjustability round out the features of the VS Series.

Input Characteristics: (at 130 Watts)

Operational Input Ranges:
(User Selectable)
1. 70-140Vac-50 to 440 Hz (see note 4 on page 9)
2. 140-280Vac-50 to 440 Hz (see note 4) (200-400Vdc)

Input Protection

Overcurrent: 2-line fusing
Inrush Current: 15 Amps peak (triac controlled)

Under/Overvoltage Shutdown Threshold Level:
(non-operational protection mode)
55 Vac/150 Vac (110 Vac in)
110 Vac/300 Vac (220 Vac in)
130 Vdc/425 Vdc (300 Vdc in)

Transient Withstand Capability (8 ms)
(non-operational protection mode)
155 Vac (110 Vac in)
310 Vac (220 Vac in)
450 Vdc (300 Vdc in)

Safety/EMI Filtering
UL478
VDE 0730 Par. 2P
CSA C22.2
FCC Docket 20780
VDE 0871

Input I/O Isolation:
2500Vac

Output Characteristics

Voltage Tolerance: 5-5.5V (adjustable)
Main Output Adjust/Remote Sensing:

The 5V output can be operated up to a maximum of 5.5Vdc either by manually adjusting the potentiometer and/or automatically via remote sense. (see note 5)

Regulation
Line: 0.4% (MAX) all outputs
Load: 0.4% (MAX) - 15% to 100% load on 5V
Load: 0.4% (MAX) - 12 (15)V
Cross: 0.4% (MAX) all outputs - 15% to 100% load on 5V
Cross: 0.4% (MAX) all outputs - 0-100% load on 12 (15V)

Ripple & Noise (PARD):
.25% Vout (VRMS)
1.0% Vout (V pk-pk)
all outputs from 90-140/180-240Vac

Temperature Coefficient:
0.02%/°C 5V output
0.05%/°C 12 (15)V outputs

Transient Response:
Recovery to 1% within 500 micro-seconds for load change of 25% - all outputs

Maximum Output Power:
150W from 0°C to 40°C
Linearly derate from 150W to 130W from 40°C to 50°C
Linearly derate from 130W to 65W from 50°C to 71°C
(available power, based on no external heat sinking)

Minimum Load:
2 Amps on the 5V output

Isolation Capability:
All outputs independent and floating up to 300Vdc with respect to chassis ground

Output Protection

Overcurrent Protection:
Power foldback overcurrent protection set at 160W; short circuit overcurrent protection on all outputs

Overvoltage Protection:
Automatically resettable crowbar on 5Vdc output set at 6.25V ±10%

Reverse Voltage Protection:
100% of rated current on all outputs

Overshoot:
None on turn-on, turn-off or power down

Holdup Time (130W):
> 30ms at 115 or 230Vac
> 20ms at 100 or 200Vac
> 10ms at 90 or 180Vac

Control Characteristics

Power Fail Signal:
Negative true signal when input falls below 90/180Vac. Output goes to the potential of the negative side of the 5V output (see note 2 on page 3).

Remote Shutdown:
TTL compatible, isolated from input by 2500Vac, 10mA, sink; negative or positive true (5V) signal actuates power down (see note 2 on page 3).

Overtemperature Control:
Automatically resettable linear power foldback circuit designed to keep the chassis below 105°C. Under all conditions of load, line and operating temperature.

Parallel Operation:
Parallel operation of up to three 5V outputs via a P.C. mounted strap and two wire interconnect between units

Switching Frequency:
40 kHz ±10%

Ambient Temperature

Operating: 0°C to +71°C
(see maximum output power spec for derating information)

Storage: (non-operating)
-40°C to +85°C

Efficiency

>75% over 2:1 input range (at 130 watts)

Mechanical Characteristics

Weight: 4.3 pounds
Cover: Expanded metal cover is provided

Mounting: 2 surfaces

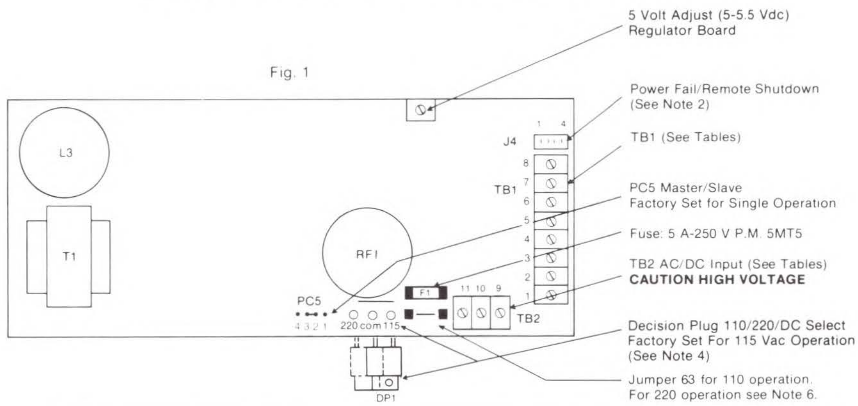
1. 10.5" x 5" (26.7 cm x 12.7 cm)
2. 10.5 x 2.5" (26.7 cm x 6.4 cm)

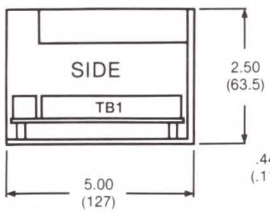
Ordering Information

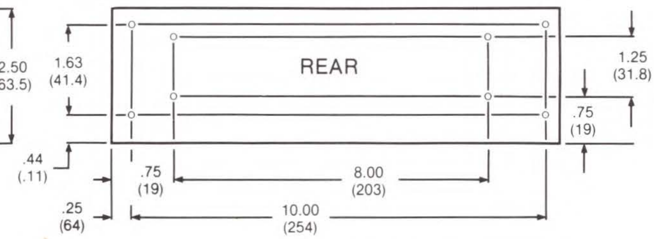
OUTPUT VOLTAGE (Vdc)	OUTPUT CURRENT (A)	MODEL NUMBER (by input voltage range)	
		70-140 Vac	140-280 Vac/ (200-400 Vdc)
		TRIPLE OUTPUT	
5/12/12* 5/15/15*	15/4/4* 15/3/3*	VS34-2300 VS35-2100	VS34-2300 VS35-2100
		SINGLE OUTPUT	
5 12 15	30 12 10	VS11-3000 VS12-1200 VS13-1000	VS11-3000 VS12-1200 VS13-1000

*OUTPUTS 1/2/3

Application Notes/Dimensions







Output (TB1)

Pin	Function	VS34 2300	VS35 2100
1	+Vdc out	12	15
2	-Vdc out	12	15
3	+Vdc out	12	15
4	-Vdc out	12	15
5	+Sense*	5	5
6	+Vdc out	5	5
7	-Vdc out	5	5
8	-Sense*	5	5

*See note 5

Input (TB2)

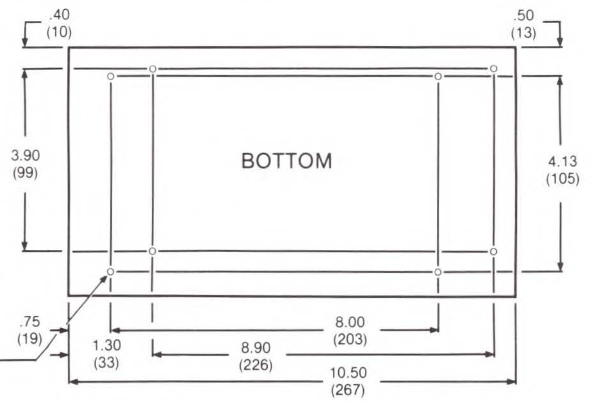
Pin	Function
9	Chassis Gnd
10	AC Input Hi*
11	AC Input Lo*

*See note 4

Power Fail/Shutdown (J4)

Pin	Function
1	Power Fail Hi*
2	N/C
3	Remote Shutdown Hi
4	Remote Shutdown Lo*

*See note 2



Mounting Holes
Hardware #6-32 x 1/4" Max-16 Places

Notes:

1. Dimensions shown at ±0.05 inches (±1.3mm)
2. The Common connection for power fail is -5Vdc out (TB1 pin 7). The remote shutdown common is isolated from input and output common
   The mating connector is Molex. Series 2695
3. All outputs are floating and may be referenced (+) or (-).
4. 110/220Vac (200-400Vdc) selectable by a decision plug (see fig. 1, DP1) **Caution-DC input in 220 volt position only.**
5. If remote sense terminals are not used, they should be shorted to their respective 5Vdc output terminals (note exception for parallel hookup). Jumpers are installed at the factory for local sense.
6. For 220Vac operation
   1. cut jumper W63
   2. reposition the decision plug to the 220V position
   3. replace f1 & f2 with the appropriate value (see fuse selection table)

Mounting Holes are Compatible with **Boschert OL/XL 130 and L.H. Research TTM 23 Models.**

FUSE SELECTION TABLE

Suggested Manufacturer/ Model Number	Rating	Size	Use
BEL 5ST5 (IEC listed)	5A @ 250V	5 x 20mm	220Vac International
BEL 5MT5 (UL & CSA listed)	5A @ 125V	5 x 20mm	220Vac Domestic

SEMICONDUCTOR CIRCUITS, INC.
49 RANGE RD., WINDHAM, N.H. 03087 (603) 893-2330 TWX (710) 366-0505

Signals & Noise

Revise our list of IEEE-488 manufacturers

Despite efforts to publish an accurate list of IEEE-488-instrument suppliers (EDN, September 1, pg 233), we missed several companies in this fast-growing field. Make the following additions and changes to complete that list.

Bering Industries Inc
747 E Brokaw Rd
San Jose, CA 95112
(408) 298-8552
Circle No 744

Winchester- and floppy-disk subsystems

Daytronic Corp
2589 Corporate Pl
Miamisburg, OH 45342
(513) 866-3300
Circle No 745

Data-acquisition, measurement and control systems

EG&G Ortec
100 Midland Rd
Oak Ridge, TN 37830
(615) 482-4411
Circle No 746

Data-acquisition and analysis systems

Eventide Clockworks Inc
265 W 54th St
New York, NY 10019
(212) 581-9290
Circle No 747

Digital delay lines, harmonizers, digital-signal processors, signal generators

ILC Data Device Corp
105 Wilbur Pl
Bohemia, NY 11716
(516) 567-5600
Circle No 748

Synchro/resolver angle indicators and simulators, data-bus adapters

Address change:

Kinemetrics
True Time Div
3243 Santa Rosa Ave
Santa Rosa, CA 95401
(707) 528-1230
Circle No 749

Time and frequency instruments

National Instruments
12109 Technology Blvd
Austin, TX 78759
(512) 250-9119/(800) 531-5066
Circle No 750

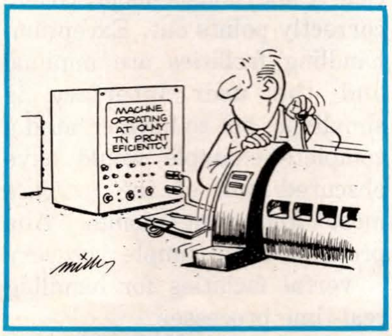
Interfaces, testers, networks

Is Ada a good choice in process-control uses?

Dear Editor:
The article, "Solve process-control problems with Ada's special capabilities" (EDN, June 23, pg 143), is a poor example of both an Ada program and a process-control application. The Ada program contains several design and coding errors, and the functions that the program tries to implement are inadequate for the application.

Program-design errors exist in the COLLECTION_OF_SENSORS, RECORDING_DEVICE and TIMER tasks. In COLLECTION_OF_SENSORS, no initial values are provided for the HIGH_LIMIT and LOW_LIMIT in each SENSOR_RECORD. Thus, the program makes it possible to ENABLE a sensor with no limit values, causing unpredictable program behavior in the sensor scanning loop.

Also in COLLECTION_OF_SENSORS, raw sensor data presumably appears in memory-mapped I/O ports as integer values in the 0 to 200 range. However, these values are defined to be of a data type with a range of 0 to 65,535. If a value greater than 200 should ever appear (because of sensor or I/O-port malfunction), the conversion of this value to a value of type SENSOR_VALUE will fail, raising a CONSTRAINT_ERROR exception. No handler



is provided by the program for this exception or for possible exceptions raised by the DEVICE_IO package in the RECORDING_DEVICE task.

The TIMER task has two functions to perform every 15 min: It must produce a sensor status log and turn on a system alarm light if the COLLECTION_OF_SENSORS task does not respond within 5 sec. A problem results from this design because if the output device that receives sensor-status data the hangs up, both the TIMER and COLLECTION_OF_SENSORS tasks wait forever, thereby stopping the system. And the system alarm light won't turn on, because in Ada, the delay statement applies to the time to accomplish the rendezvous, not the time to complete the task.

The article also contains program-coding errors. In the main program, the statement

```
entry POST_FAULT_IN_SENSOR;
```

should be

```
entry POST_FAULT_IN_SYSTEM;
```

and in TIMER, the statement

```
ALARM.POST_FAULT_IN_SENSOR;
```

should be

```
ALARM.POST_FAULT_IN_SYSTEM;
```

Also, in RECORDING_DEVICE, the statement

```
DEVICE_IO. PUT (OF_STATE);
```

should be

```
DEVICE_IO.PUT(OF_SENSOR);
```

and in ALARM, the statement

```
for LIGHT use (OFF=>16×00#,
ON=>16×FF#);
```

should be

```
for LIGHT use (OFF=>16×0000#,
ON=>16#FFFF#);
```

Finally, the main program contains no exception handler for CONSTRAINT_ERRORS as required by the text.

Although the author probably wanted to keep the example simple, it is too simple to be very realistic. Furthermore, for process-control engineers, who spend only a small percentage of their time programming, Ada would not be a good choice for this application because it requires a high degree of programming sophistication to correctly solve this problem. A better choice would be one of the many monitoring systems offered by process-control companies, either in the form of small, dedicated alarming data loggers or as a function of larger process-control systems.

Paul D Griem Jr
Technical Consultant
The Foxboro Co
Foxboro, MA

Author's reply

Mr Griem's letter raised two major points regarding the article: inadequate functionality and some coding errors. First, I fully agree with him that the example is not completely realistic; it was never intended to be. To demonstrate principles of programming in the large, one must make simplifications to show the principles in the small. The example I presented is clearly not robust—as Mr Griem correctly points out. Exception-handling facilities are minimal and the user interface is simplistic, but to have created a complete example would have obscured one of the article's most important points: Ada provides some simple yet very powerful facilities for handling real-time processes.

Continued on pg 28

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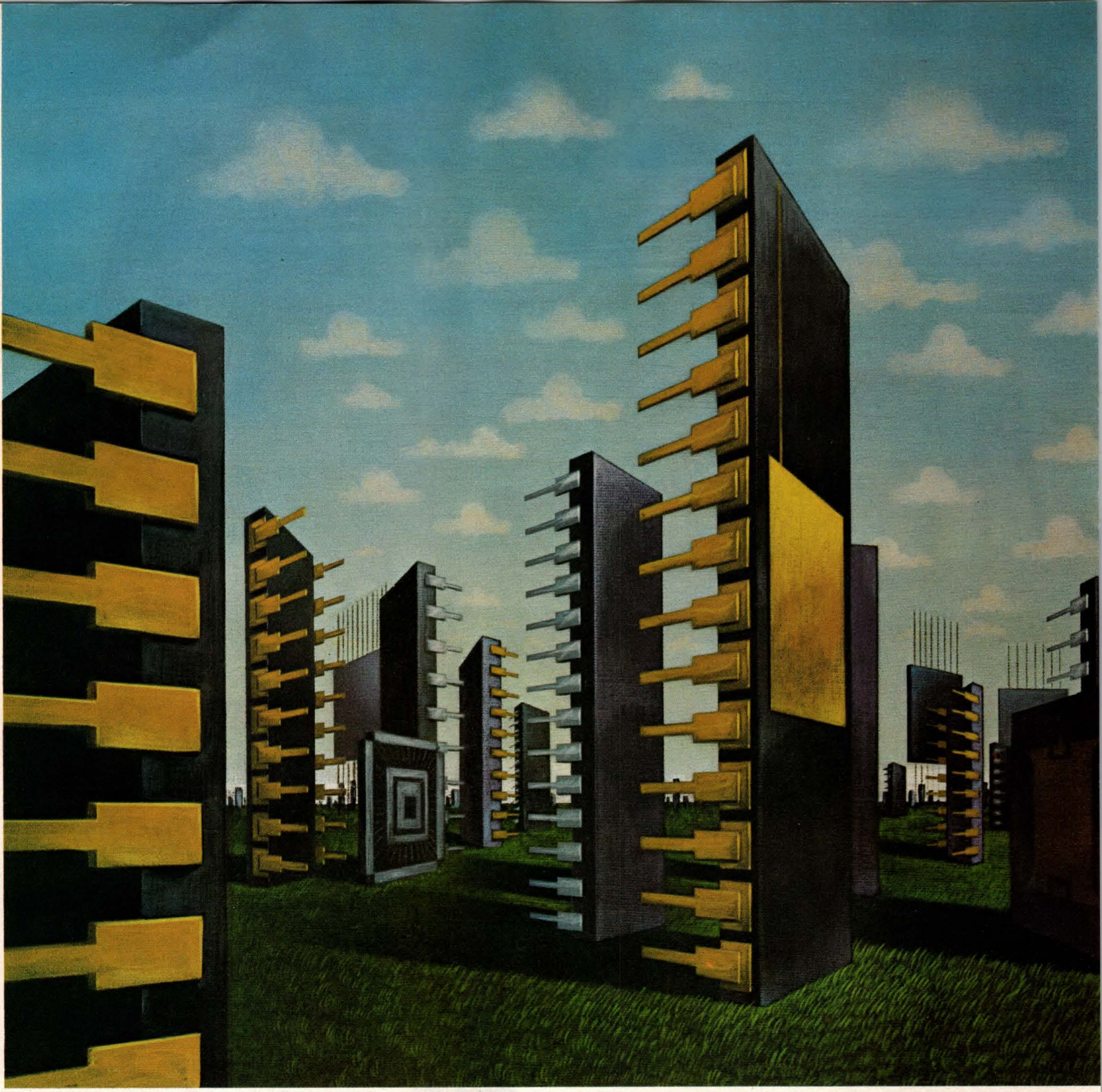
LSTTL I/O Compatible	YES	YES	YES	NO	NO
Guaranteed LSTTL Fanout	30	30	30	1	10
Typ. gate delay (ns)	3	3	5	>30	5
Typ. operating current (mA)	100	<1	<1	<1	<1

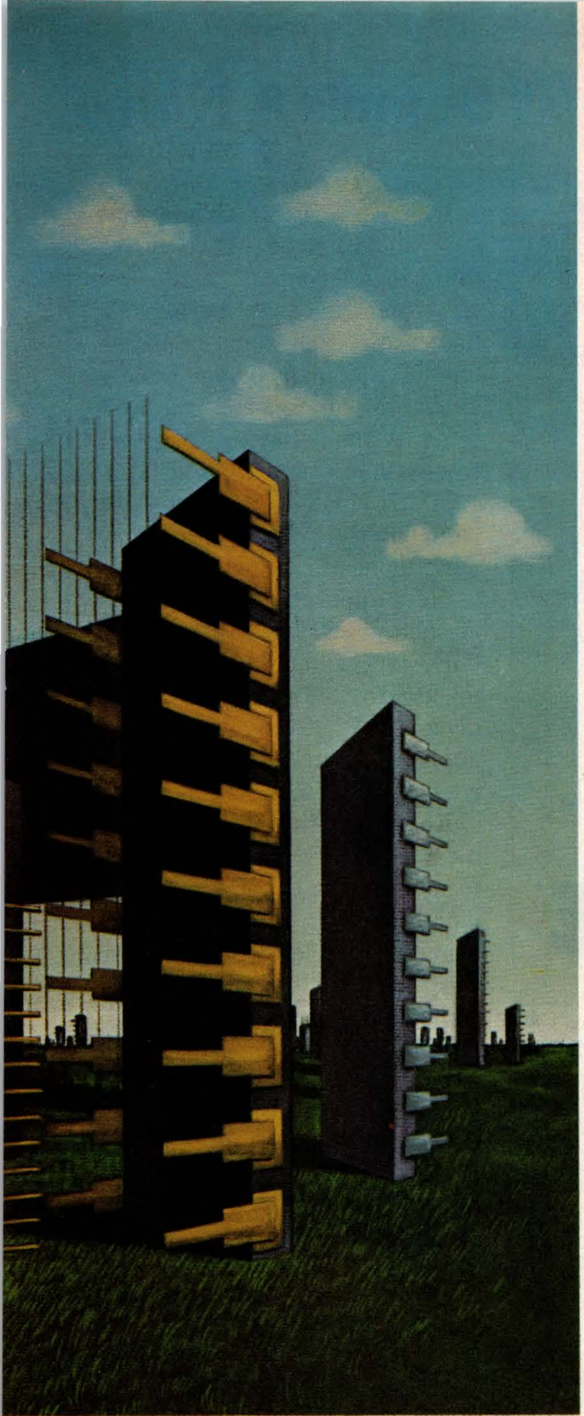
Device types now available from stock: 137, 138, 139, 237, 238, 239, 240, 241, 242, 243, 244, 245, 373, 374, 533, 534, 540, 541, 563, 564, 573 and 574 — commercial and military.

CIRCLE NO 9



TESTING, TESTING, TESTING.

SERIES 10 AND 20 PRODUCTION TEST SOLUTIONS



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When you're looking for a solid, single-source solution to a wide spectrum of production test problems, look no further than Fairchild.

MULTIPLE CHOICES.

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And the 20 MHz Fairchild Series 20.

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Dedicated to delivering all the production test flexibility you need. Today. And tomorrow.

The system you choose depends upon your production test needs.

The Series 10 offers a flexible, cost-effective solution to the testing of LSI devices with speeds up to 10 MHz. It gives you high throughput, high uptime and low cost.

Series 10 options include an algorithmic pattern generator for testing memory devices and an expandable timing system for testing more complex devices. Mag Tape and Disk add program development, debug capability and easy transfer of programs from other Fairchild systems to the Series 10.

The Series 20 is designed to help you accurately test VLSI high-speed devices such as microprocessors, gate arrays, peripheral chips and memories that run as fast as 40 MHz and up to 120 I/O pins.

The Series 20 is available with high-speed or high-voltage test heads. Options include a memory test pattern generator and error logger. Mag Tape and Disk. And the Sentry® Analytical Graphics Enhancement (SAGE), a time-slashing debug tool.

Like the Series 10, the Series 20 is backed by fifteen years of ATE software development. They also incorporate Fairchild's M³ operating system and FACTOR programming language.

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SINGLE-SOURCE SOLUTION

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For more on the Series 10 and 20 production test solutions, call or write: Fairchild Test Systems Group, 1601 Technology Drive, San Jose, CA 95115, (408) 998-0123, Ext. 2296. Fairchild Camera and Instrument Corporation.

CIRCLE NO 10

Signals & Noise

I agree with Mr Griem that Ada would not be a good choice for process-control engineers. He suggests that perhaps a better approach would be to use one of the many commercially available process-control systems, without having to resort to creating a new application in Ada. It makes no sense to reinvent the wheel with every new application, however—Ada is quite applicable to the design of such process-control systems (GE, for example, has studied its use to control an automatic oven, and other groups are applying it to similar process-control problems).

Regarding the coding errors, most of Mr Griem's comments focus on a lack of exception-handling code. I chose not to provide complete facilities for the sake of simplicity. His comment regarding initial values for the HIGH_LIMIT and LOW_LIMIT of each sensor points out an oversight on my part. In the body of the task COLLECTION_OF_SENSORS, the declaration of SENSOR can be modified by adding an initial aggregate value:

Continued on pg 32

NEXT TIME

EDN's December 17 issue is our 16th semiannual Product Showcase, an invaluable compendium of information on the most noteworthy new-product introductions of the past 6 months. You won't want to be without this fact-filled reference issue, which is organized into seven key product areas:

- Components and hardware
- Computers and peripherals
- ICs and semiconductors
- Instruments
- Power sources
- Products from Europe
- Software

EDN: Everything Designers Need

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CIRCLE NO 13

SEEQ SETS A NEW STANDARD FOR 5V E^2 ROM.

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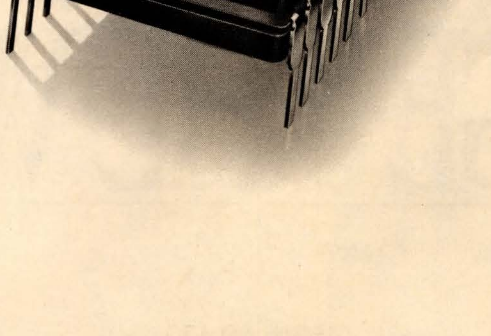

It's the standard that eliminates the remaining obstacles to E^2 design. Because 5 volt Electrically Eraseable ROMS are finally available and cost effective.

This ad and $9.95 will get you a 5213 5 volt E^2ROM at any Schweber Electronics location.* And that's just the beginning. For orders placed after July 1, 1983, we'll meet your production needs (25,000 units minimum) at that same price. So you'll have enough fast (350 ns read, 1 ms single byte write), reliable (10,000 cycle write endurance), and cost effective 5 volt E^2ROMs to implement any application you can think of.

Here's a good reason to think of one right away.

$9.95 can get you a Porsche.

SeeQ will award a 1983 Porsche 944 to the winner of our 5213 16K E^2 Application Contest.

Imagine an application that demands E^2 s combination of nonvolatility and in-circuit alterability. Like remotely programmable PBXs. Process control monitors that compensate for mechanical wear. Or juke box controllers that tell servicemen to replace worn records.

Whatever your idea, build it, test it, and send us the schematic before January 10, 1983. If your design is judged the best, you'll drive to your next project meeting in a Porsche 944.

Complete rules and entry forms are available from your local Schweber Electronics location. Or contact SeeQ Technology, 1849 Fortune Drive, San Jose, California 95131. Telephone (408) 942-1990.

But whether you win or not, designing with our 5 volt 5213 will put you in the driver's seat. Because in setting standards for E^2ROMs, SeeQ is more than a little ahead.

In fact, it's no contest.

*Offer limited to two 5213s per person. See Schweber for details.

SEEQ

CIRCLE NO 14

Signals & Noise

```
SENSOR : SENSOR_GROUP :=
SENSOR_GROUP'(others =>
  (HIGH___LIMIT  => SENSOR_
VALUE'LAST
  LOW___LIMIT  => SENSOR_
VALUE'FIRST,
  VALUE        => SENSOR_
VALUE'FIRST));
```

Using this form, Ada requires that every component of SENSOR be given a value; thus, the initial VALUE is set to the smallest possible SENSOR_VALUE.

Grady Booch
US Air Force Academy
Colorado Springs, CO

For additional data on thermometers...

Dear Editor:

I regret that the following reference was inadvertently omitted from my article, "Evaluate sensor tradeoffs in digital-thermometer design" (EDN, September 29, pg 115): Erdi, George, *Thermometer Applications of the REF-02*, AN-18, Precision Monolithics, 1976.

While at PMI, Mr Erdi designed the REF-02 and rigorously described its performance as a temperature sensor.

Sincerely yours,
Wes Freeman
Applications Engineer
Teledyne Semiconductor
Mt View, CA

Your turn...
EDN welcomes your comments, pro or con, on any issues raised in the magazine's articles. Address letters to **Signals and Noise Editor, EDN, 221 Columbus Ave, Boston, MA 02116.** Names will be withheld upon request. We reserve the right to edit letters for space and clarity.

Nichicon Capacitors vs. Switching Regulators

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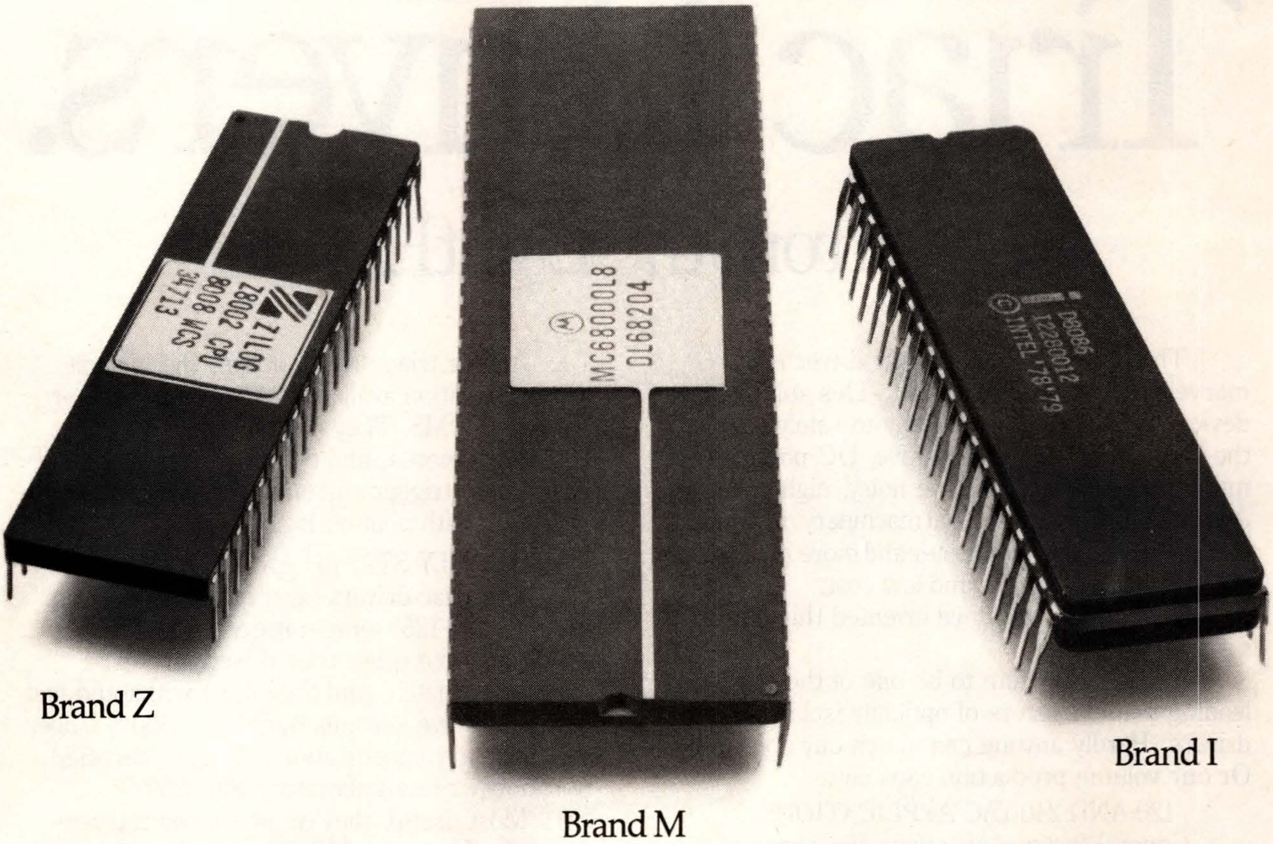
CIRCLE NO 18

Born.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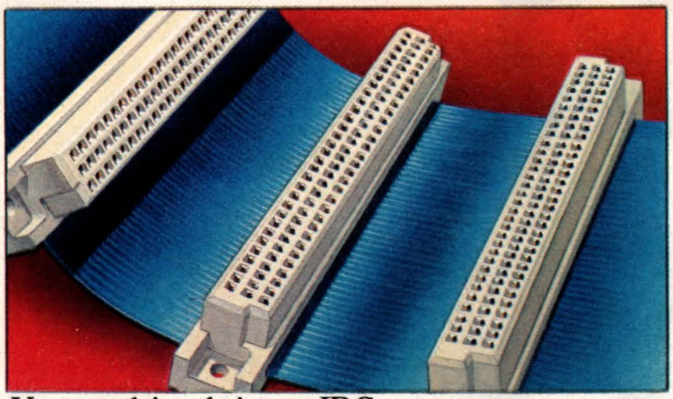

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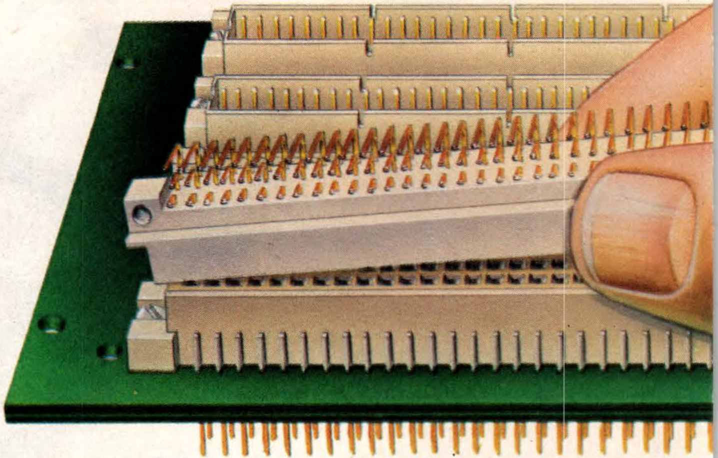

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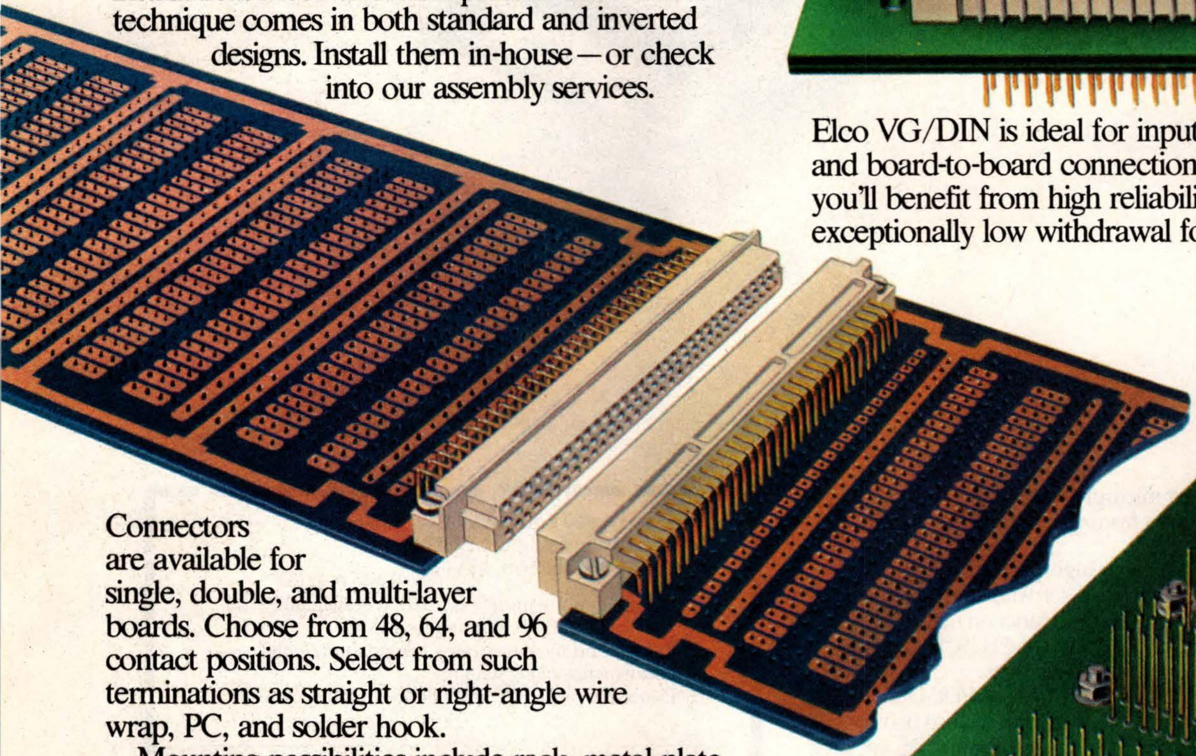

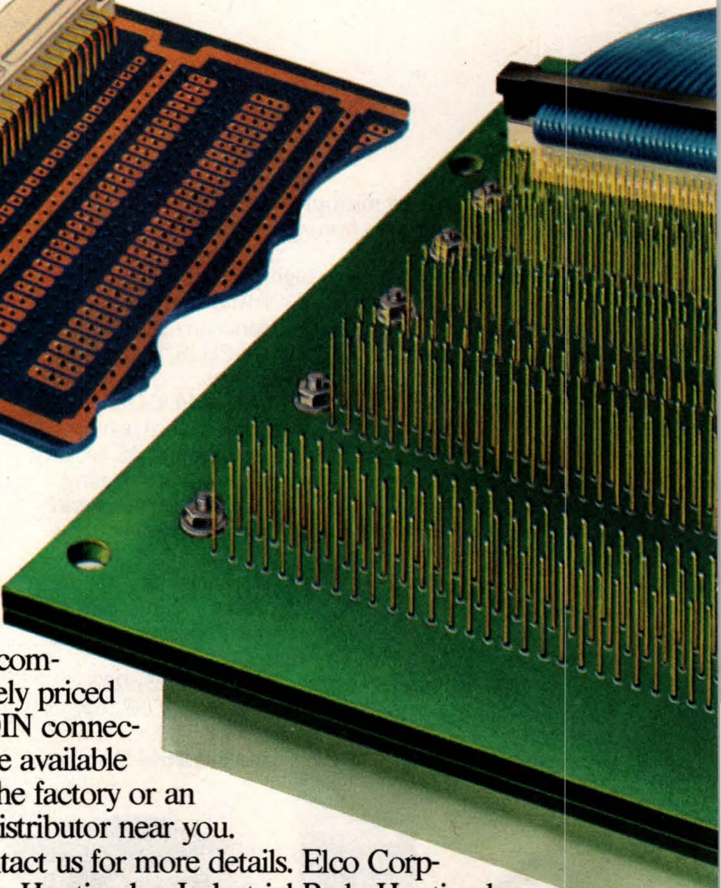

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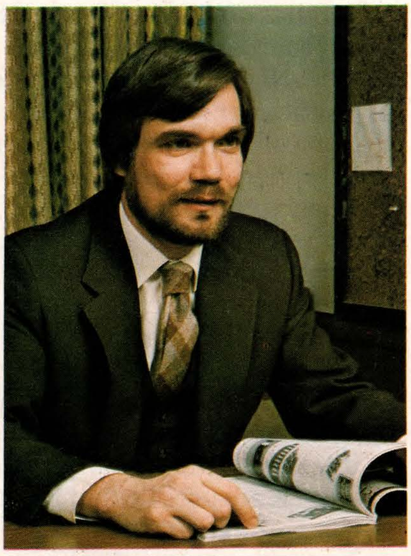
CIRCLE NO 19

Editorial



Use semicustom logic to achieve a design edge

At a recent EDN Design Conference on semicustom logic, approximately 5% of the attendees indicated that they incorporate that technology in their designs. And because those present presumably had high interest in the topic, it's safe to assume that an even smaller percentage of the engineering community as a whole is taking advantage of semicustom design approaches.

Some recent product introductions, however, point out that EEs not yet familiar with semicustom logic should quickly pull their heads out of the sand or risk getting left far behind by the competition. For example, Seeq Technology, which participated in the race to bring the first Ethernet controller chip to market, used custom programmable-array logic (PAL) to bring its design from conception to working prototypes in 11 months. Thus, this dark horse was the first firm to enter what should prove to be a narrow market window (several similar introductions are imminent).

The trend to semicustom logic affects not only chip designers, but systems designers as well. Star Technology's recently introduced FT-100 32-bit floating-point array processor, for instance, uses 180 gate-array devices on three 12×12-in. boards, replacing an estimated 12 to 15 boards of standard logic. The firm claims a 4:1 price/performance improvement over other array processors (thanks to reduced materials, manufacturing and testing costs). It also notes that sophisticated CAE software allowed its designers to simulate circuits sufficiently to obtain working parts on the first try, rather than struggle through the multiple development cycles required with standard logic.

Producing similar savings, Metheus uses 26 PAL devices in the processor board for its λ750 workstation (see pg 81 in this issue) to eliminate a pc board of logic and thereby cut user price by an estimated $1800. Ironically, although the system uses PAL devices, it aids EEs in designing full-custom, standard-cell and gate-array circuits.

The message should be clear: Competitive pressures will force your company to turn to semicustom logic to achieve shorter design cycles in developing less expensive, more reliable products. EDN's coverage of this technology will aid you in understanding the basics and keeping track of what's available, but smart EEs won't delay in also getting hands-on experience. That way, they can assess the benefits of semicustom logic as soon as they begin their next design project.

Paul G Schreier
Editor

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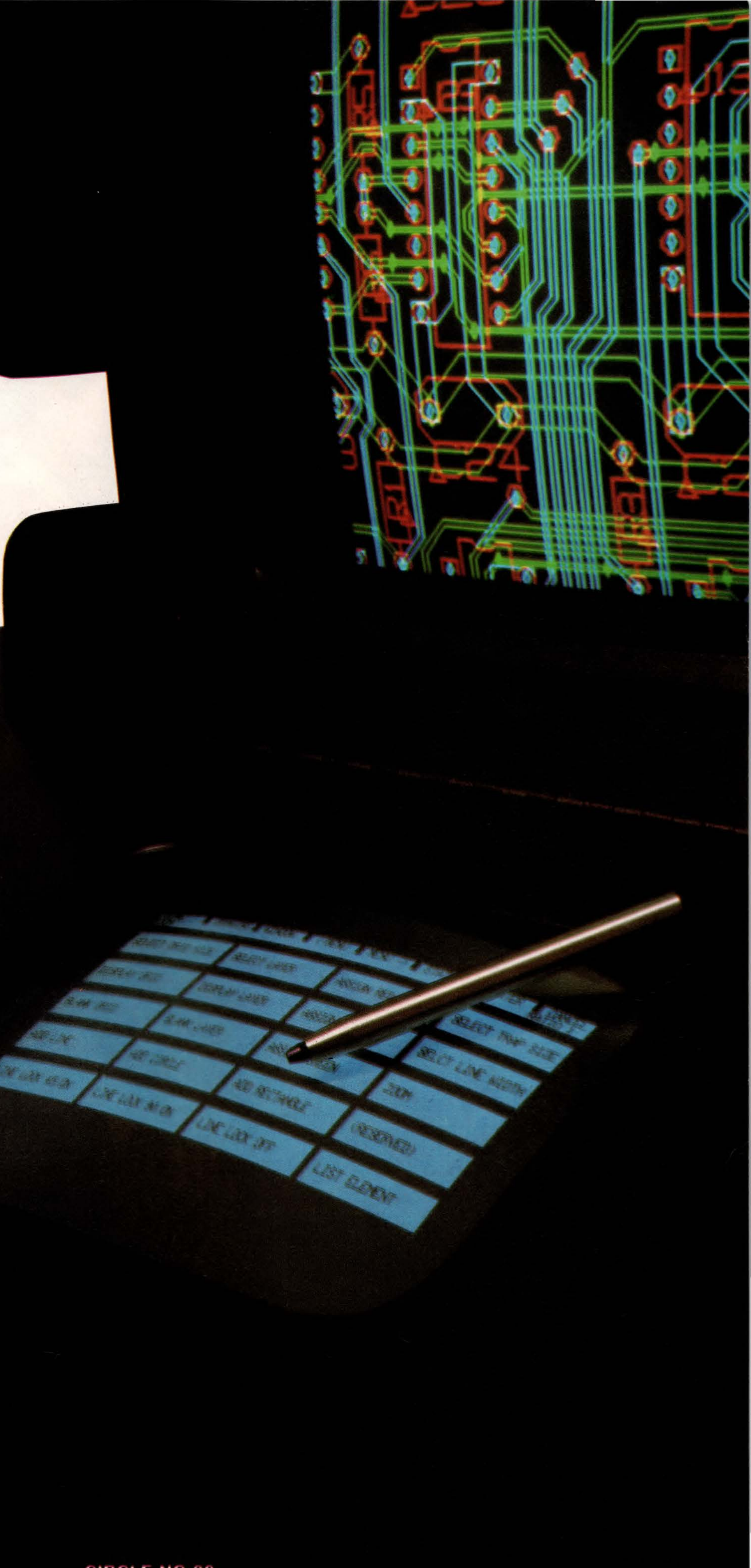

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```
4100 REM      SET UP PS5010
4110 PRINT @22:"INIT;VPOS 11.7;IPOS 0.5;OUT ON"
4120 REM      SET UP DC5010
4130 PRINT @20:"INIT;TER LO;AUTO A;PER;SEND"
4140 INPUT @20:P
4150 PRINT @20:"MAX?;MIN?"
4160 INPUT @20:M1,M2
4170 A=M1-M2
4180 PRINT @20:"RISE;SEND"
4190 INPUT @20:R
4200 PRINT @20:"FALL;SEND"
4210 INPUT @20:F
```

Our Common Codes and Formats ensure compatible data transfer between instruments—which IEEE-488, by itself, does not.

And basic to the Tek GPIB concept is a commitment to design instruments that are eminently compatible, not just with controllers, but with people who use them.

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Common Codes and Formats keep commands clear and consistent. Their English-like programming language makes bus control exceptionally simple, even for the non-technical programmer. Writing systems software is easier, programs more efficient and self-documenting.

The command set is in "standard engineering English" matching the abbreviations on instrument front panels. As is shown above, readable mnemonics in the command string set up the PS 5010 Programmable Power Supply and the DC 5010 Programmable Universal Counter. In line 4110 we set the PS 5010 positive supply for 11.7 volts with an 0.5 amp current limit, and turn the supply output on. In lines 4130 through 4210 we measure the period, amplitude, risetime, and falltime of a signal and set them equal to P, A, R, and F, respectively.

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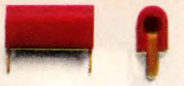

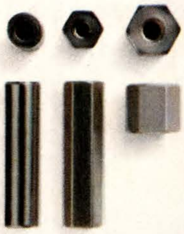

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CIRCLE NO 21

Multibus-compatible analog I/O cards serve diverse system needs

Edward R Teja, Western Editor

To circumvent the headaches of interfacing a computer to analog equipment, more and more digital designers are turning to the latest analog I/O cards—especially those serving the Multibus. These cards simplify the analog-design task a great deal—merely matching card performance to your system needs takes care of all your analog design requirements.

This design simplification brings with it some specification difficulties, though: Multibus-compatible analog I/O cards provided by 14 manufacturers offer a wide range of price levels to choose from. For example, Burr-Brown's MP-8608 8-channel analog-input card costs $375; at the other end of the price spectrum, the militarized SECS 80/732 analog-input card from EMM/Sesco costs $4700.

Finding the outer limits

Moreover, your choices center on more than price alone; performance also can vary widely. A typical analog-input card furnishes 16 differential or 32 single-ended channels. But many accommodate additional analog channels on the same card through optional multiplexers. And in some cases, cards can be combined in parallel to get the full number of channels needed.

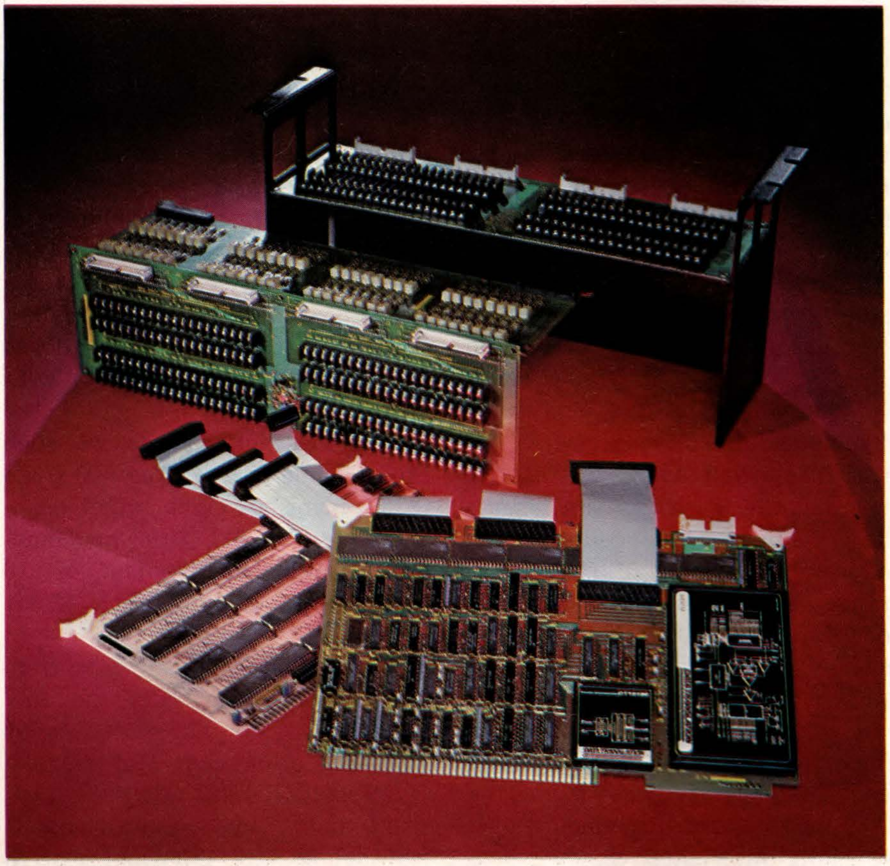
ADAC Corp's $895 710-RL low-level data-acquisition system, for example, comes with eight or 16 input channels. In addition, it provides a connector that allows you to daisy-chain $750 Model 710-RX 16-channel expansion modules to reach 128 input channels.

Data Translation, on the other hand, furnishes the DT3772 Series I/O expansion cards, which increase the usefulness of the firm's DT3752 Intelligent Analog Peripherals (IAPs). Various versions offer input ranges designed to match particular analog-signal ranges.

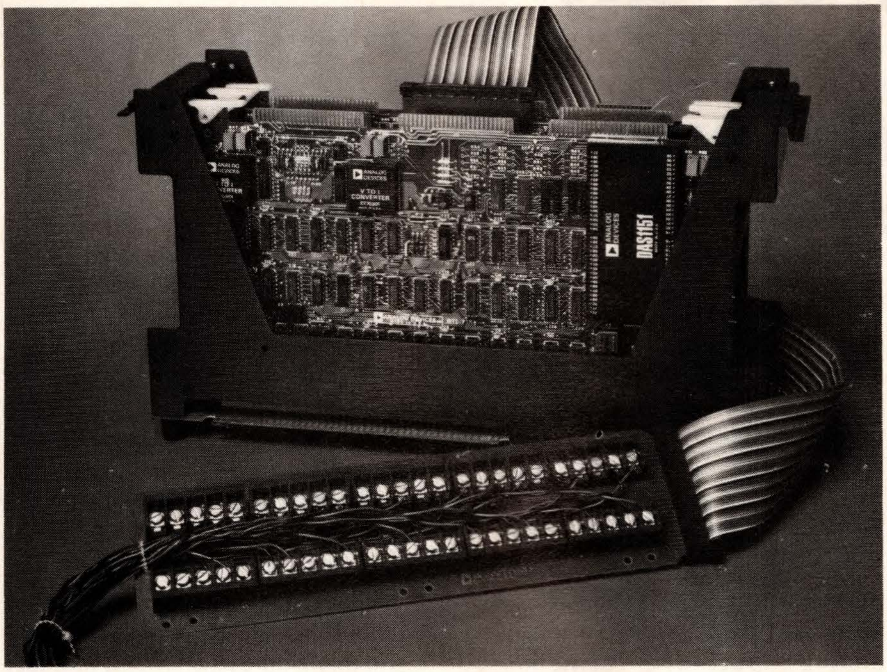
For example, Model DT3772 ($595) expands the $1895 DT3752 from 16 to 64 single-ended inputs (32 differential) that handle ±10V input ranges; it also provides as many as eight analog outputs. Model DT3775 ($695) suits low-level inputs, furnishing an $1895 Model DT3755 IAP with as many as 12 10-mV to 10V differential inputs with ±250V common-mode-voltage noise isolation.

Thus, if you can't find precisely the board that suits your design needs, look to the selection of expander cards and analog preprocessors most manufacturers offer. They can equip a system to handle even more inputs, provide more outputs or accommodate higher or lower level signals than the data sheets hint at.

In addition, some boards feature special circuits that increase design flexibility. On-card dc/dc converters, for example, come standard on some analog boards but are optional on others. With such a dc/dc converter, analog cards that typically require ±15V as well as the 5V



Put large numbers of analog channels *into a computer at low cost per channel with Data Translation's DT712 Series. Its members provide 128 single-ended or 64 differential input channels on one card—more if you use an expander.*



Memory-mapped extended addressing *over a 24-bit range is a prime feature of Analog Devices's RTI-711 analog-input board. It suits the board for use in systems with 16M bytes of memory.*

that the Multibus provides can operate with no additional power.

All converters aren't alike, however. Some offer extremely low noise; others provide just the required high voltages with reasonable regulation (1%) at low cost. And still others furnish both high dc voltages and regulation for the 5V supply. An analog-card vendor can help determine which you need.

The missing trend setter

The de facto standard for analog-input boards is Intel's iSBC 711; for analog-output boards, the iSBC 724; and for I/O combinations, the iSBC 732. This status proves rather ironic on two counts.

First, although several major manufacturers—including Datel-Intersil, Data Translation, National Semiconductor, EMM/Sesco (whose boards are militarized versions of the Intel products) and Distributed Computer Systems — produce boards that are plug compatible with the Intel iSBC 700 Series, those boards are far from standardized. And second, although companies continue to make boards to match Intel's standard, Intel itself has discontinued its iSBC 700 Series.

Examine the first consideration in more detail. Although the manufacturers claim iSBC 700 Series compatibility, each can point to innovations that make its boards more powerful, easier to use or more cost efficient than the Intel units.

Consider the RTI-700 Series, announced last month by Analog Devices. In addition to touting the RTI-711, -724 and -732 boards ($580, $445 and $670 (10), respectively) as direct replacements for the industry-standard 711/724/732 boards, the series's data sheets describe memory-mapped extended addressing over a 24-bit address range—a feature that suits the boards for unlimited use in 16-bit systems that might require as much as 16M bytes of memory.

In comparison, National Semiconductor's $634 BLC-711 has a 12-bit address range. Yet both it and the ADI boards furnish 16 single-ended or eight differential channels (expandable to 32 and 16, respectively), a crystal-controlled pacer clock, 60-dB common-mode rejection, ±10.24V common-mode voltage and system accuracy of 0.05% FSR±½ LSB with unity gain.

Datel-Intersil's analog-output card, meanwhile, designated the SineTrac ST-716, is hardware compatible with the iSBC 724 standard. One configuration, the 4-channel version, is also software compatible; both versions use 16-bit-resolution DACs versus the 12-bit-resolution units employed in other 724-compatible cards. The card provides a 20-bit address range. A 4-channel ST-716 with dc/dc converter costs $895.

You can see, then, that the practice of adding capabilities makes a de facto standard difficult to maintain; the standard instead defines a subset of a card's capabilities. Generally, however, it's safe to assume that "711/724/732 compatible" means that a board works with Intel's single-board computers.

Going piggyback

What about Intel's "abandonment" of its own standard? With the discontinuance of the iSBC 700 Series, Intel's current card offerings add analog I/O capability to a processor system via the piggyback iSBX connector available on some single-board computers. The approach is attractive, because it frees the Multibus from dealing with analog processing.

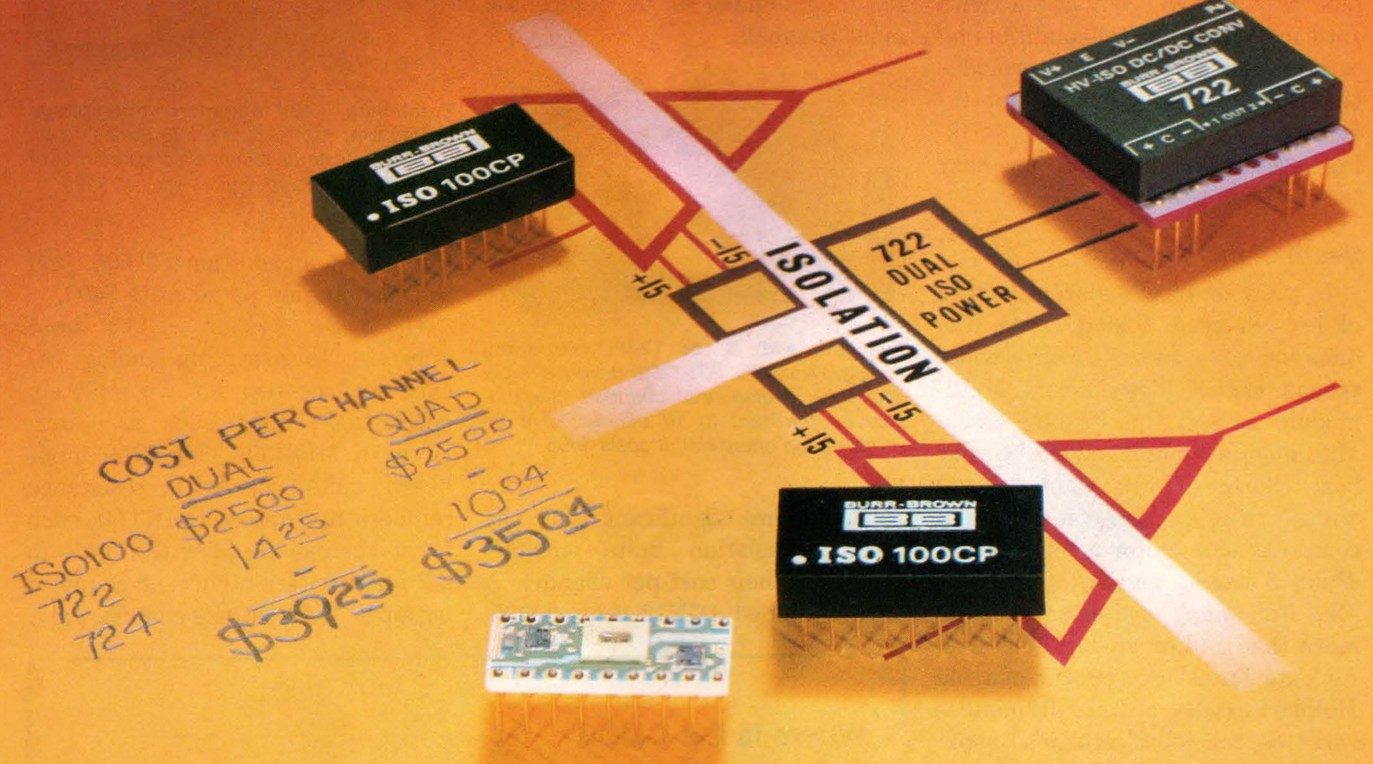
Intel has introduced two such Multimodule boards: The iSBX 328 ($750) furnishes eight output channels; the iSBX 311 ($610) accommodates eight differential or 16 single-ended inputs with 12-bit resolution.

Another alternative comes from Zendex Corp, currently the only supplier of input and output capability on a single Multimodule: Its Model ZBX-324 ($291) features two 0 to 10V analog-input channels (through an 8-bit ADC) and two 0 to 10V outputs (from an 8-bit DAC).

To use a Multimodule analog I/O

$35 Per Channel Analog Isolation Cost

Here's How You Get It



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Model	Non-Linearity % (max)	Input Offset Voltage mV (min)	Input Offset Voltage Drift μV/°C (max)	Price 100's* from
ISO100AP	0.4	0.5	5	$25.00
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This new design - featuring proven technology, fewer parts, smaller size and low cost - gives you improved reliability and performance ... just what you'd expect from the undisputed leader in isolated signal conditioning products.

ISOLATED DC/DC CONVERTERS

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722: Dual DC/DC Converter with 15 volts input; two bipolar outputs of ±15V, ±40mA each. Continuous 3500V isolation (8000V test). $28.50 in 100's* - only $14.25 per channel.

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CIRCLE NO 22

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card, merely plug it in on any single-board computer with an iSBX bus connector. Each 2.5×3.7-in. card gets its power, ground and control signals via the piggyback bus and is pin compatible with Intel's iCS 910 signal-conditioning/termination panel, which provides termination and current-loop-to-voltage conversion resistors, making system modification an easy task even in the field.

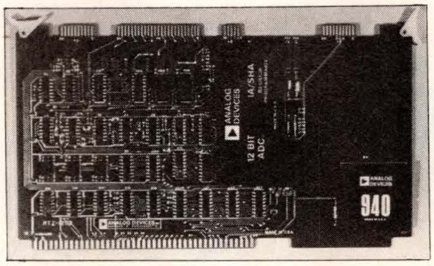
Death of the big card?

In view of Intel's discontinuance of its full-sized analog cards, the question of a move toward widespread use of piggybacked Multimodules arises. And in some cases, Multimodules might indeed be your best choice—if you want to add simple analog functions to a computer or monitor a few preconditioned analog signals, for example. But many systems must do more than add-on analog functions. As Data Translation president Fred Molinari points out, Multimodules won't do the job if you need sophisticated data acquisition.

The problem, according to Molinari, is one of flexibility. "There's no sensor in the world that puts out a clean signal from 0 to 10V." Because of the likelihood of an imperfect input signal, a quality data-acquisition system needs a sophisticated analog-input card, able to accommodate optional on-card signal conditioning and with software-programmable gain amplifiers. It might even have to work with a preprocessor that performs extensive signal conditioning.

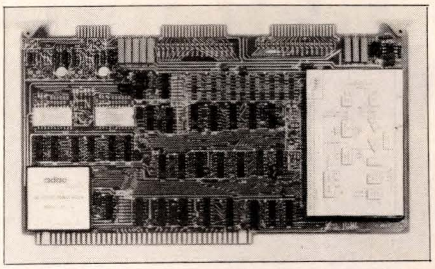
To help get large numbers of analog signals into the computer in such cases, Data Translation has introduced a line of high-density input cards. Model DT712 provides 128 single-ended or 64 differential input channels on one card. And adding the DT713 or -715 expander card results in 512 single-ended or 256 differential channels.

To accommodate signal conditioning, the family includes a series of panels and plug-in cards. The cards, including the DT706, furnish passive signal conditioning, and the panels provide screw terminals and ground connections for as many as 128 single-ended or 64 differential input channels.



Available with 8- or 12-bit resolution, *Analog Devices's RTI-1202 provides eight differential analog-input channels (expandable on the card to 16 differential or 32 single-ended channels). It costs $495.*

Even more significant than the Data Translation units' channel density is their cost per channel. A fully equipped DT712 costs $1495; the DT713, an additional $1595. And the termination panel costs $400.



Furnishing ±40V common-mode-voltage protection, *ADAC Corp's 735 Series 12-bit analog-input cards features a choice of 35- or 100-kHz conversion. Prices start at $395.*

In some systems, the best approach to providing analog I/O capability centers on a completely specialized board such as Burr-Brown's MP8430. This $750 input board suits use with resistance temperature detectors (RTD); each input channel supplies the 0.55- to 2.2-mA excitation current required by an RTD to set the channel gain.

Where is the CMOS?

Although CMOS devices are emerging as a major force in the designer's world (EDN, September 29, pg 88 and June 24, 1981, pg 89), few of the analog I/O cards in this survey are CMOS. In fact, the only totally CMOS card comes from CMOS specialist Diversified Technology, whose systems find use in harsh environments such as oil rigs.

CMOS boards furnish all the traditional advantages of CMOS components: low power consumption, immunity to noise, wide power-supply range, wide operating-temperature range and high speed. And although all of these factors are significant advantages, the high noise immunity of a CMOS integrating converter proves particularly significant: It eliminates the need for a large amount of on-card signal conditioning that might be required for an input board to work well in industrial environments.

What about price? The traditional high cost of CMOS is rapidly diminishing. A typical input card from Diversified Technology costs $1145.

The key to Diversified Technology's use of CMOS, however, lies in its provision of a total CMOS system: CMOS analog circuits working in conjunction with a CMOS computer. Unfortunately, the world of Multibus systems includes few CMOS CPU cards. Diversified Technology offers an interface that adapts its analog board to a TTL-level bus, but the match seems ungainly. Therefore, until more CMOS μCs appear on the Multibus, the market for CMOS analog I/O cards will remain small.

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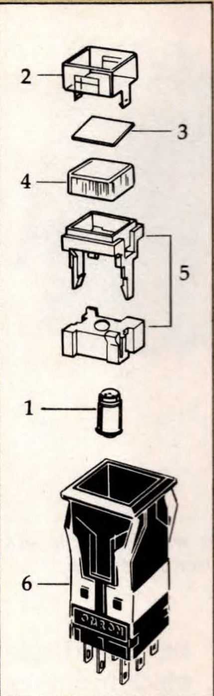

A unique LED array (1) broadens and intensifies brightness (visibility up to 200 feet) without sacrificing low-power benefits (uses as little as 15 milliamps).

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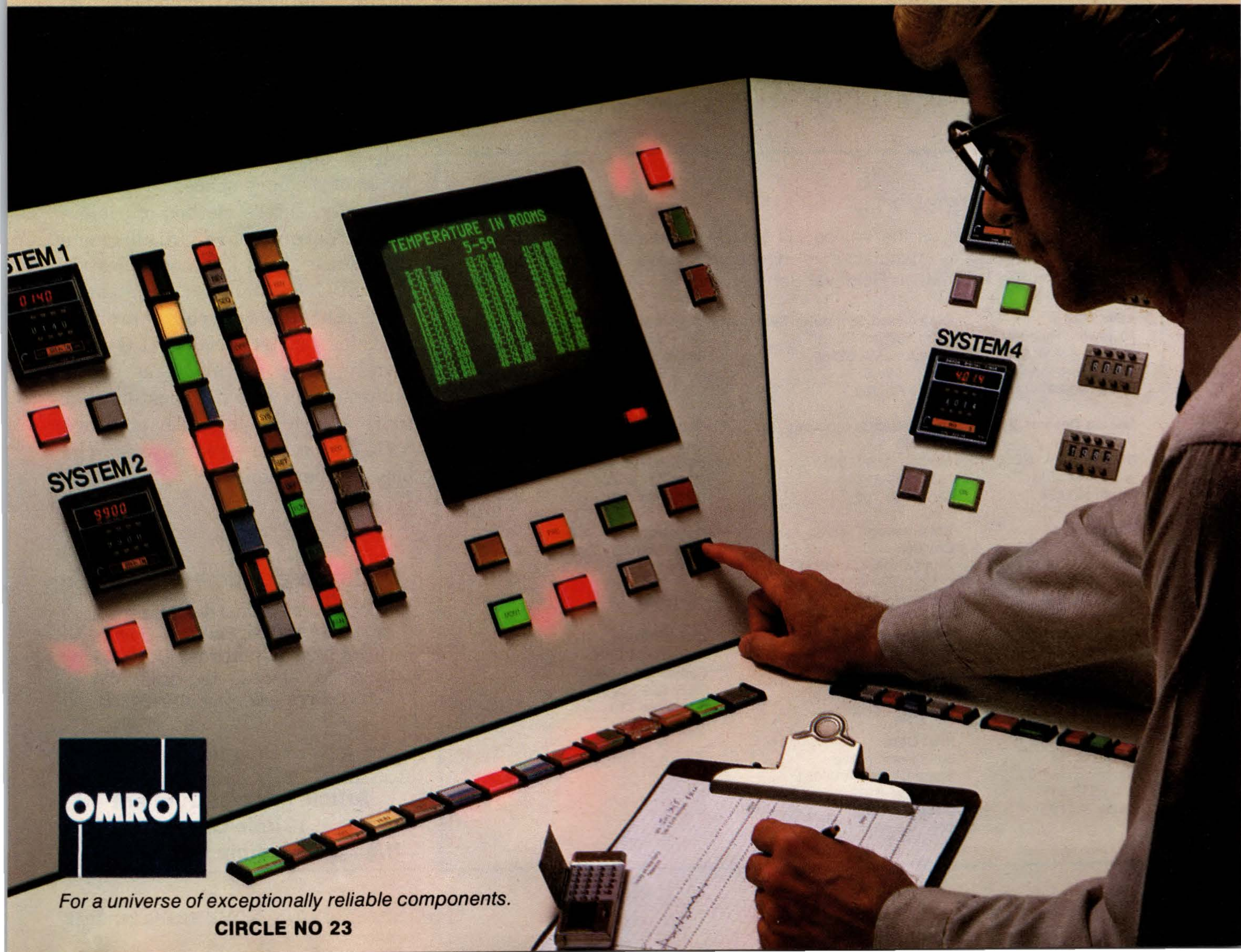
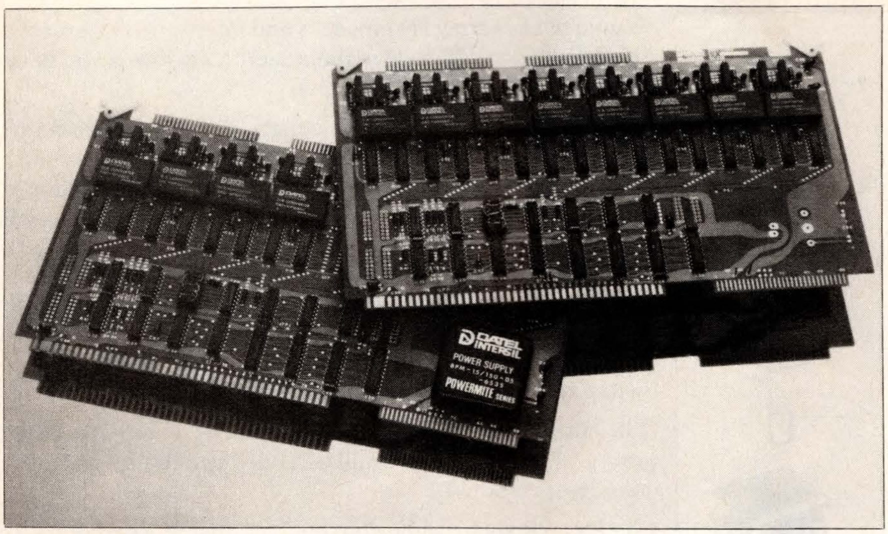


For a universe of exceptionally reliable components.

CIRCLE NO 23



Get 16-bit resolution *on as many as eight analog-output channels with Datel-Intersil's SineTrac ST-716. A typical 4-channel board with on-card dc/dc converter costs $895.*

The board both accommodates the inputs from the sensor and becomes part of the sensor circuitry.

Multimodules aren't always the most cost-effective approach to interfacing with a noise-free analog environment, either. A better alternative might be MegaLogic Corp's GAB-1/MN, which furnishes four analog-input channels with 12-bit resolution and costs only $395. Thus, choosing the Multimodule alternative depends as much on the piggyback approach's convenience as on cost factors: Big cards aren't dead or even dying.

Besides coming in a variety of sizes and featuring specialized signal conditioning, analog boards are also keeping pace with designers' needs by becoming smarter. Robotrol Corp's $1210 RMB 741 analog I/O card, for example, uses an on-board μP to simplify programming. You control its 12 analog outputs and 16 differential/32 single-ended inputs via 8-bit registers, specifying the operating parameters and strobing the data into the appropriate register.

ETI Micro's 8131 input card, on the other hand, trades off simple operation for flexibility—it operates as an intelligent Multibus slave. This unit's on-board 8085 μP controls 16 differential analog inputs; the board converts the analog signal into a 12-bit-wide bit stream and stores it in 2k bytes of dual-port RAM. The bus master can then access the data directly. Setting hardware switches allows you to locate the RAM over 1M bytes of memory space.

Finally, Intel's method of achieving greater board intelligence makes use of the iSBX modules via the iSBC 88/40 board. This measurement-and-control computer provides smart analog I/O—you merely plug as many as three Multimodules into it to customize it to your own system. An on-board 88/10 processor coordinates the board's operation. **EDN**

For more information...

For more information on the analog I/O boards discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

ADAC Corp
70 Tower Office Park
Woburn, MA 01801
(617) 935-6668
Circle No 697

Analog Devices Inc
Box 280
Norwood, MA 02062
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Data Translation
100 Locke Dr
Marlboro, MA 01752
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11 Cabot Rd
Mansfield, MA 02048
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(601) 856-4121
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EMM/Sesco
Box 668
Chatsworth, CA 91311
(213) 998-9090
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ETI Micro
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Intel Corp
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Robotrol Corp
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Circle No 709

Zendex Corp
6644 Sierra Lane
Dublin, CA 94566
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Circle No 710

Acknowledgement

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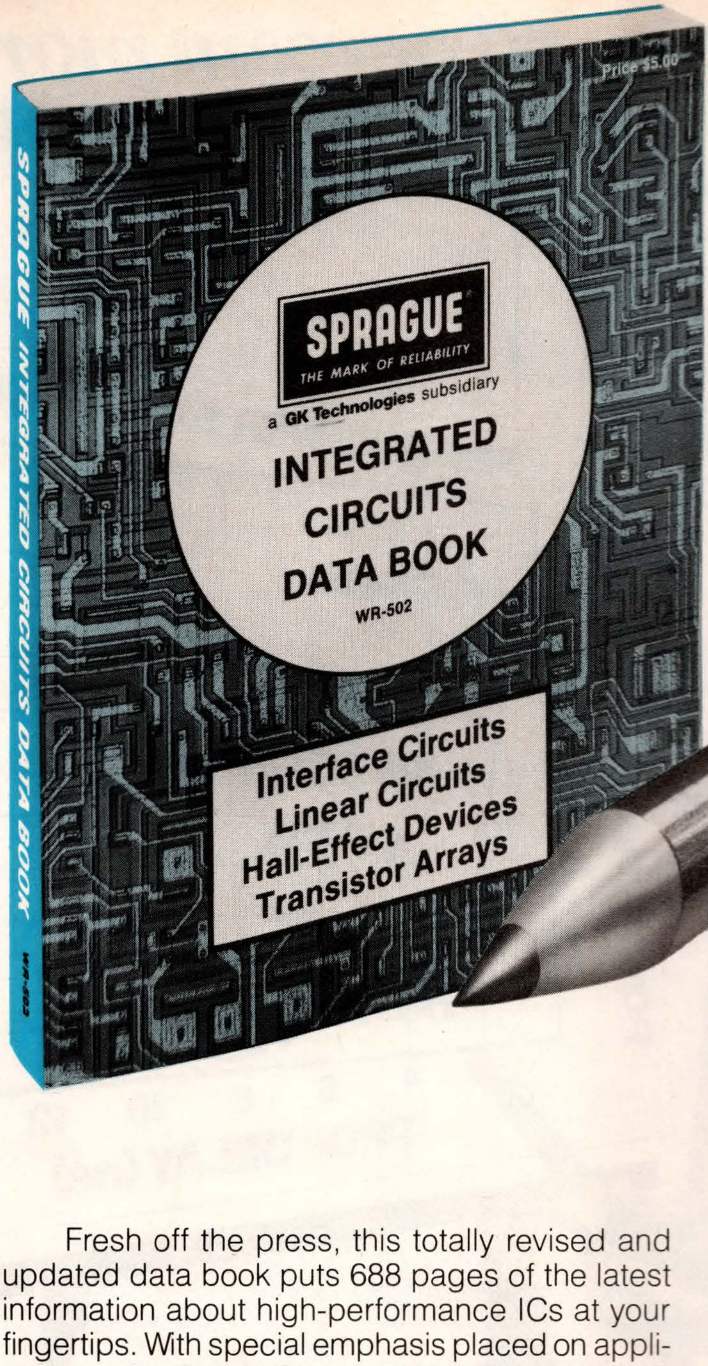

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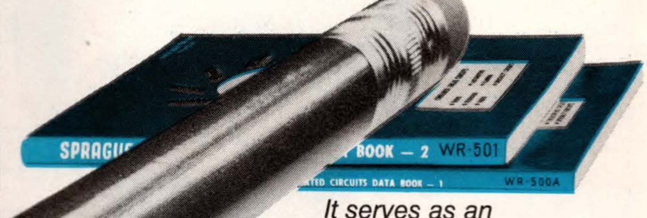

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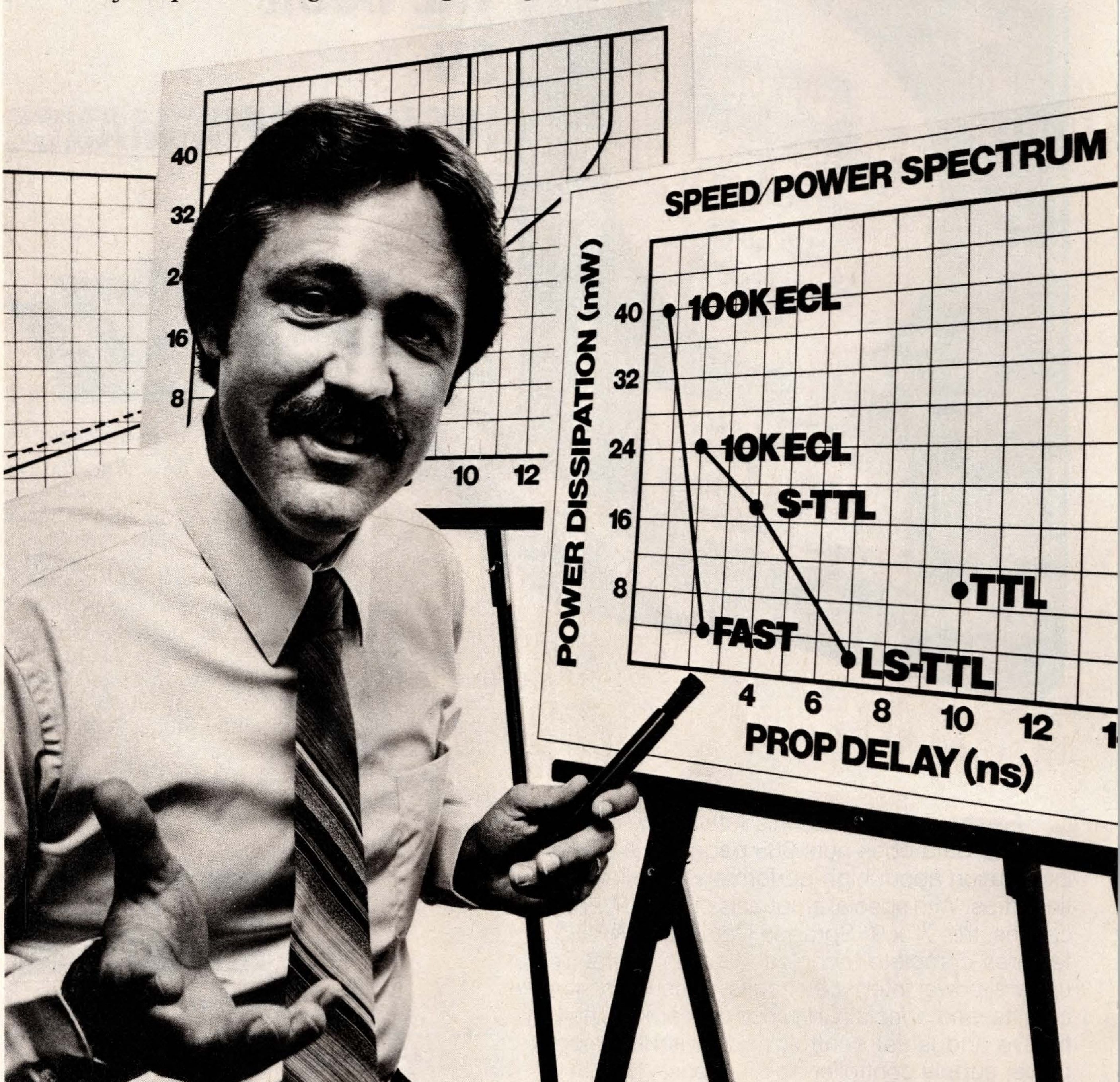

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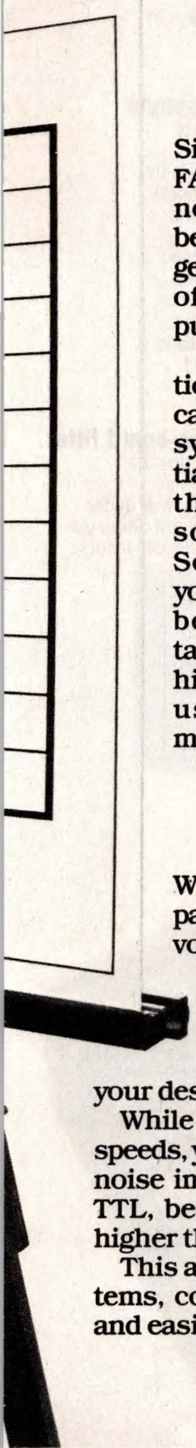

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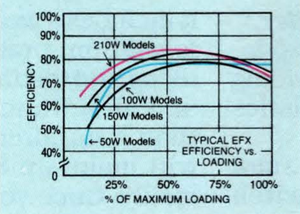

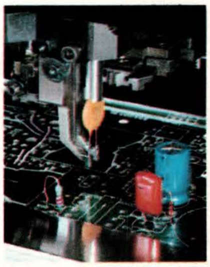
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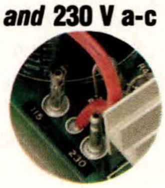

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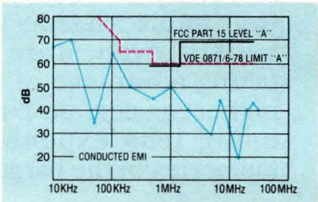
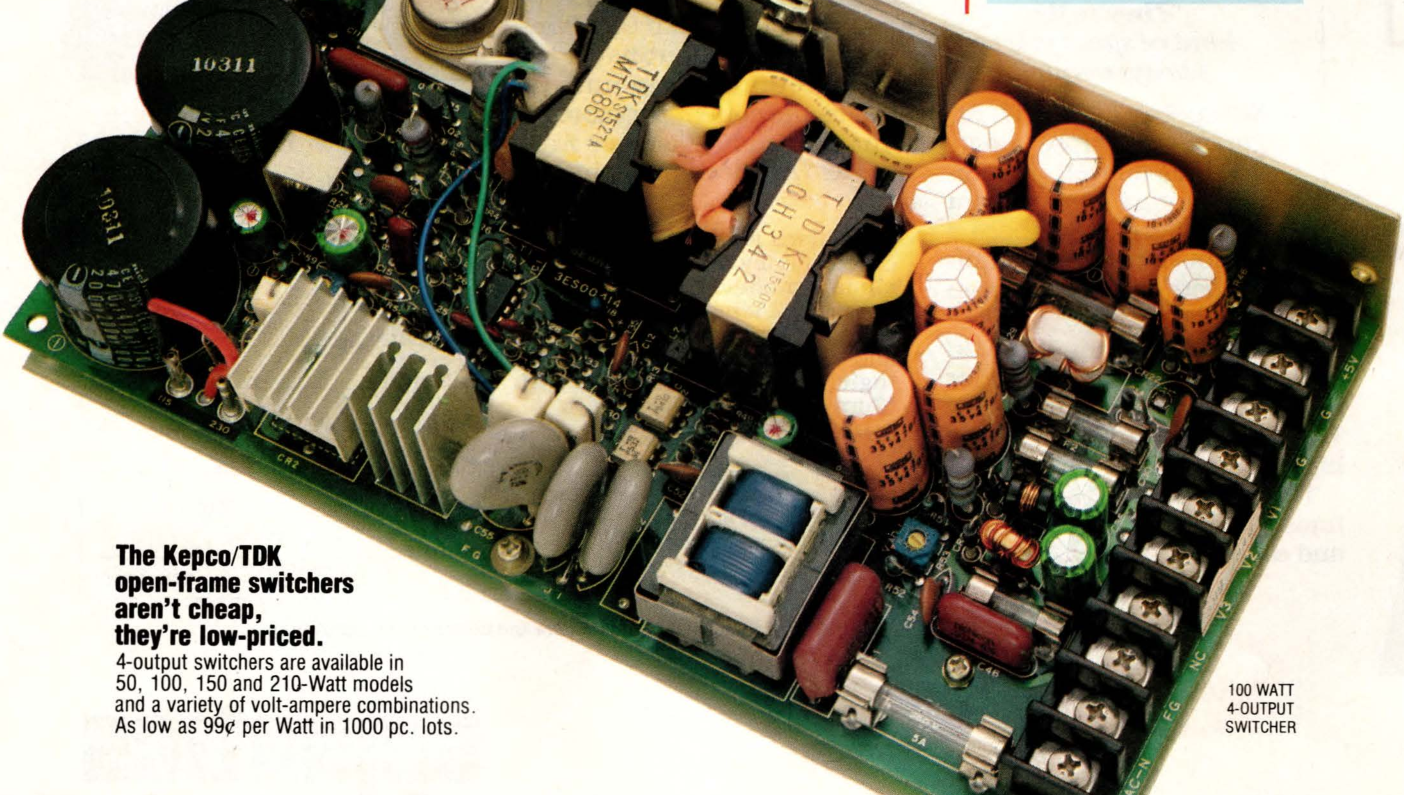


Look at the temperature rating of the capacitors: cheap ones are rated at 85°C. Good ones at 95°C. *Ours are 105°C.*



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CIRCLE NO 25

Hard-disk controller chips simplify custom interface designs

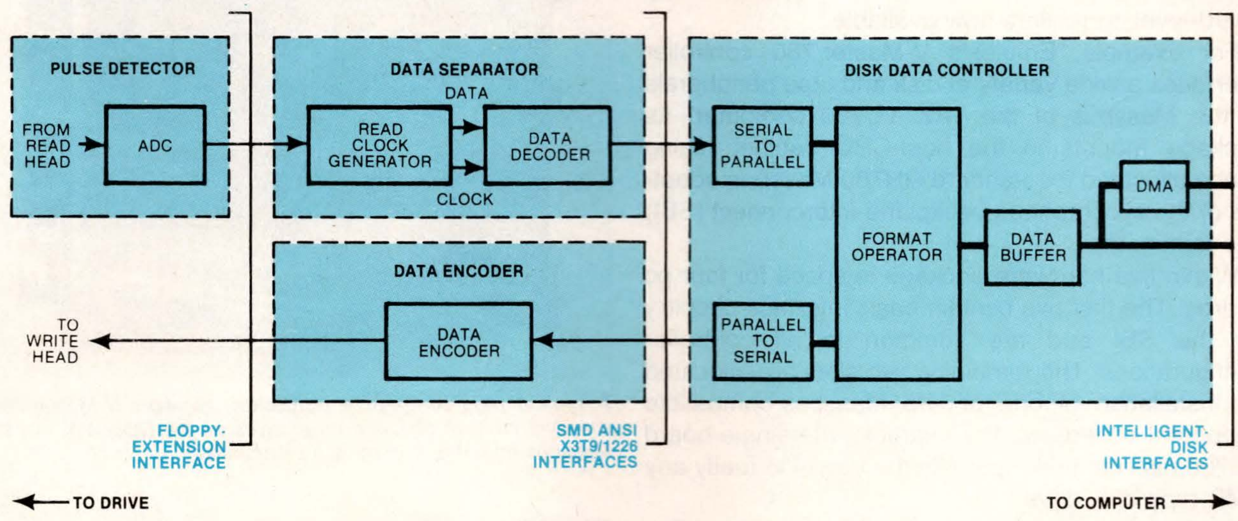
Franklin G Fink, Associate Editor

Recently introduced hard-disk controller ICs make it easier than ever to design controller-to-computer interfaces for a variety of drives—if you design by the chip manufacturers' rules. That is, if you plan to configure a custom, special-purpose hard-disk controller (perhaps one that implements a subset of the emerging SASI standard), these highly integrated chips provide capabilities that make the job relatively simple. If, however, your controller-to-computer interface must embody a system-specific standard (such as the Multibus or S-100 bus), you're still better off buying one of the many available specialized board-level controllers (see **box**, "Plug-compatible controllers interface easily").

Standards emerge

A hard-disk interface has two parts: the circuitry that joins the drive to the controller, and the circuitry that interfaces the controller to the computer. Drive-to-controller interfaces are now well defined, and the controller ICs each accommodate one or more of them. They fall into several categories:

- **ST506 (Seagate)**—Based on the 5¼-in. Winchester drive pioneered by Seagate Technology, this interface is now also implemented by many other manufacturers. It's essentially a high-performance, high-capacity version of the established 5¼-in.-floppy-disk (mini-floppy) interface. Initially, drives with the ST506 interface stored 6M bytes, but versions storing as much as 52M bytes have been announced. An ST506 controller essentially does what a mini-floppy controller does, but at a faster rate (typically 5M bps) and usually with error-correction capability.
- **SMD**—This interface is based on the Control Data Storage Module Drive, which comes in 14- and 8-in. versions and stores as much as 380M bytes. An SMD interface incorporates data-separation and data-encoding functions, not included in the ST506 interface.



Interface standardization at several levels *has simplified the job of designing some hard-disk controllers around one of the ICs now available. On the drive side, the controller must accommodate either the floppy-extension (ST506), SMD, ANSI X3T/1260 or proposed ANSI intelligent-drive interface; each of the hard-disk controller chips handles one or more of these standards. On the computer side, the controller must accommodate the SASI interface standard, one of the standardized μC buses (Multibus, STD bus, Q-bus, etc) or a custom interface you might choose to configure. (Such a custom interface might be a subset of the SASI.) Only for a custom interface or the SASI interface is it cost effective at moderate volumes to use a hard-disk controller IC; you're better off using a preconfigured interface board if your system must interface to one of the system-specific buses. Most designs, though, are probably best suited to the custom-interface approach.*

- **ANSI (ANSI X3T/1260)**—Like the SMD interface, this drive-to-controller interface includes more signal-processing electronics than the ST506 interface. The ANSI specification calls for only one clock between the drive and controller—a combined read-clock/servo-clock signal. The SMD specification, on the other hand, calls for both clocks to be simultaneously on the interface.
- **Proposed ANSI intelligent-drive interface**—This proposed standard places in the drive much of the drive-to-controller interfacing intelligence that would usually be associated with the controller. Communication occurs over an 8-bit bus, and control signals are in a high-level command language. This type of interface might not require any drive-to-controller interface circuitry.

What about the controller-to-computer half of the hard-disk interface? It, too, has been defined in several forms:

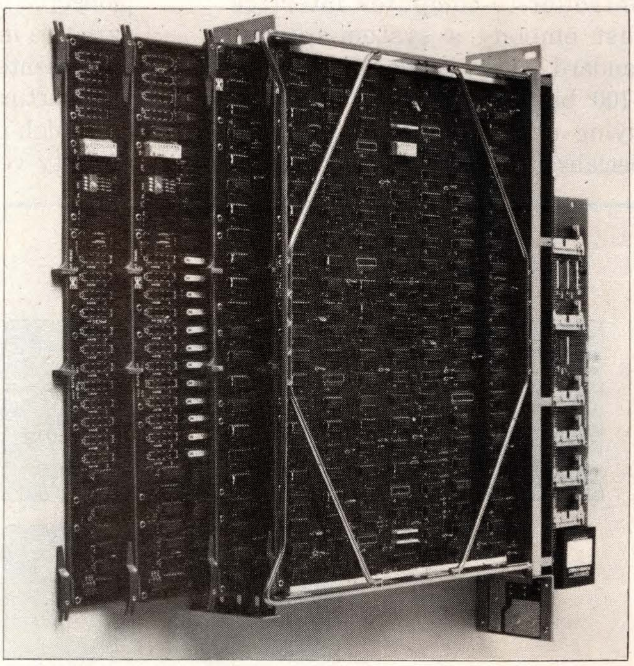
- **SASI (Shugart Associates Standard Interface)**—In this proposed standard interface for storage devices, one computer can address several SASI interfaces on the bus, and each SASI interface can select one of several devices, which need not necessarily be disk drives. The advantage of this approach is that the same interface can accommodate several types of devices—tape or hard-disk drives, for example. Another important feature is block-multiplexed operation: The ability of the controller to operate independently of the bus.
- **Plug compatible**—System-specific interfaces for the Multibus, S-100 bus, Q-bus,

Plug-compatible controllers interface easily

Although the newest hard-disk controller ICs are extremely capable, they're still not the most cost-effective approach to designing interfaces that accommodate a system-specific bus standard (Multibus, Q-bus, STD bus, etc). These interfaces call for using a large number of glue parts to comply with the bus standard; unless you're designing for very high volumes or making performance improvements to the bus, you're better off using one of the many board-level controllers now available.

For example, Emulex's V-Master/780 controller interfaces a wide variety of disk and tape peripherals to the Massbus of the VAX 11/780 computer. Its package mounts in the host-CPU cabinet, using space allocated for standard RH780 Massbus adapters or the synchronous-backplane-interconnect (SBI) bus terminator.

Within this hardware package is space for four pc boards. The first two contain basic interface circuitry for the SBI and are common to all controller configurations. The remaining two slots are allocated for installation of one or two Massbus-compatible peripheral controllers. For example, the single-board SC780 disk controller permits the use of virtually any SMD-type disk drive.



A typical plug-compatible controller, *Emulex's V-Master/780 supports multiple disk and tape drives on the DEC VAX 11/780 Massbus from one chassis in the computer.*

Another board-level controller, Data Systems Design's $2000 DSD 5215 Multibus controller/interface occupies one Multibus socket and simultaneously interfaces to a 5¼-in. Winchester drive, ¼-in. streaming-tape drive and 5¼-in. floppy-disk drive. It emulates the Intel iSBC 215 and iSBX 218 controllers and therefore provides software compatibility with Intel's RMX86 operating system. Designed with a high-speed bus for data pipelining and compatible with the IEEE-796 (Multibus) standard, this controller features noninterleaved data transfer with 8- or 16-bit transfers and on-board data separation. It supports 24-bit addressing and can take advantage of such high-performance μPs as the 16-bit 68000.

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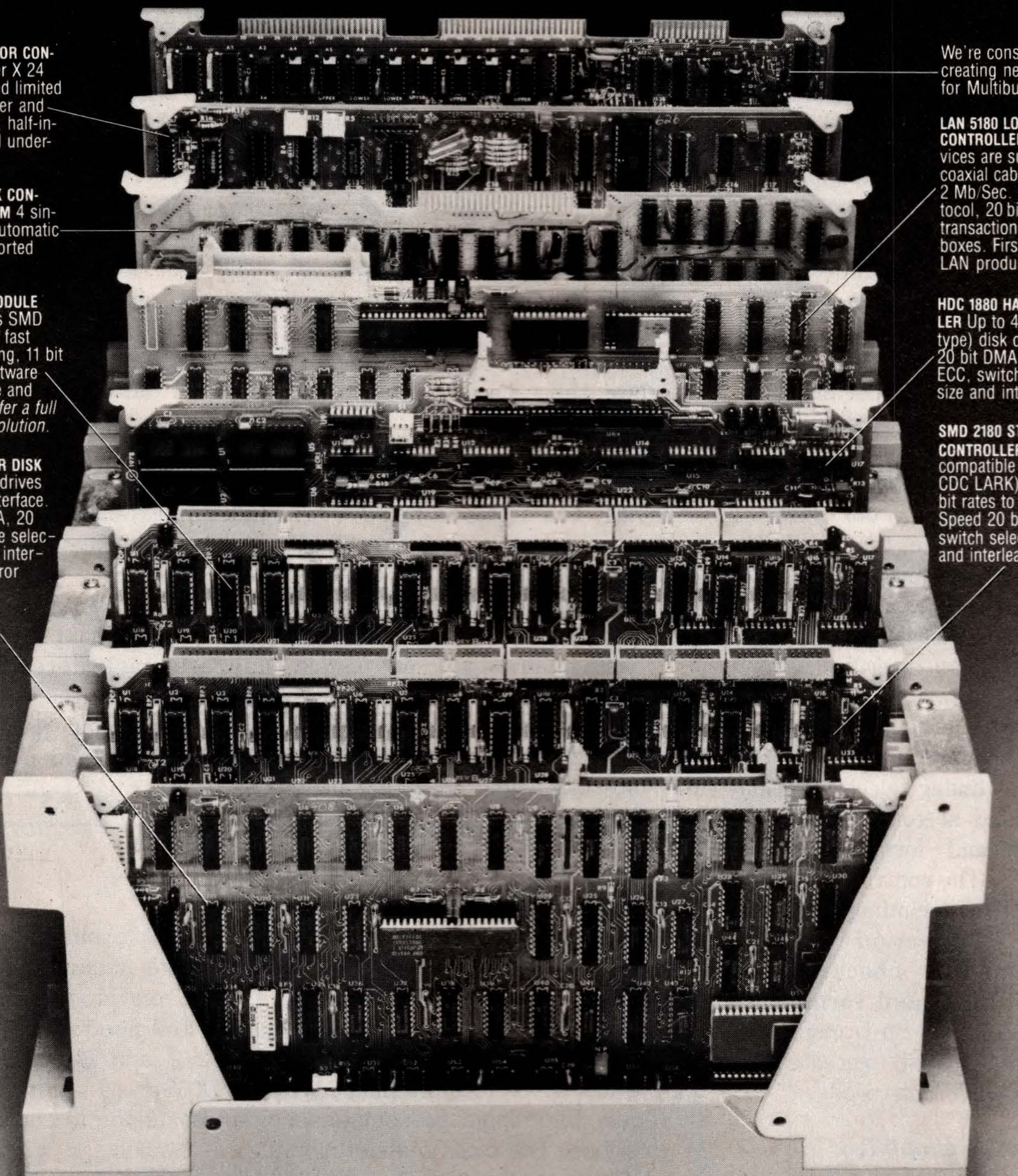

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CIRCLE NO 26

Exorbus and other buses are designed to plug into a card cage and in each case are hardware and software compatible with the bus originator's product. This type of controller-to-computer interface frequently requires many glue chips (components that provide the bus-specific signals required by the system's hardware and software). Thus, it's usually not cost effective to design your own unless you need large quantities or improved performance.

- **Custom**—In most applications, it's not cost effective to implement a full SASI interface; a simpler one suffices. Here's where the hard-disk controller chips shine: Because they incorporate all required intelligence, designing such an interface around them is not difficult. The computer merely supplies the controller with head-, drive- and cylinder-select information and sector-search, read/write and formatting commands. The controller does all the work, including providing error correction. Indeed, ECC (error checking and correction) and formatting functions remain transparent, unless you wish to create your own control microcode.

SASI interface simplified

The hard-disk controller ICs are just starting to become readily available; most are in the sampling stage. And even within this group of broadly capable products, capabilities vary.

For example, Adaptec's $165 (OEM qty) ACS5000 chip set and $325 (OEM qty) ACB5000 controller board implement the full SASI interface—the controller thus operates independently of the control bus, except when it's receiving commands or transmitting data. In this block-multiplexed mode, the controller operates at its full information-interchange capability, sharing the bus with other SASI-interfaced devices. This powerful multitasking capability was previously available only on mainframes.

Adaptec's $140 (OEM qty) ACS4000 chip set and $300 (OEM qty) ACB4000 controller board, meanwhile, implement a subset of the full SASI interface. These products lack the block-multiplexed mode and must be in control of the bus during read, write or format operations. However, don't underestimate their power. Zero-interleaved operation allows them to perform a read operation in one pass. And they also provide ECC capability and defect skipping.

If you need a low-end controller, consider Adaptec's AIC100 Winchester controller chip. It's intended for applications where minimum cost, minimum space or unique controller requirements are paramount. The device interfaces between NRZ data and host-memory-bus interface chips operating over 8-bit data and address buses.

An adaptable controller

Another capable hard-disk controller IC comes from NEC. In this μPD7261 (see pg 133 in this issue), writing a configuration command into the control register configures the control lines to be compatible with either SMD or ST506 drives.

The device's sophisticated instruction set minimizes overhead on the host μP; the μP need only load a few command bytes into the 7261 to allow all data transfers associated with read, write or formatting operations to be performed by the 7261 and its DMA controller. In addition, extensive error reporting, command verification and ECC and CRC data-error checking ensure reliable controller operation.

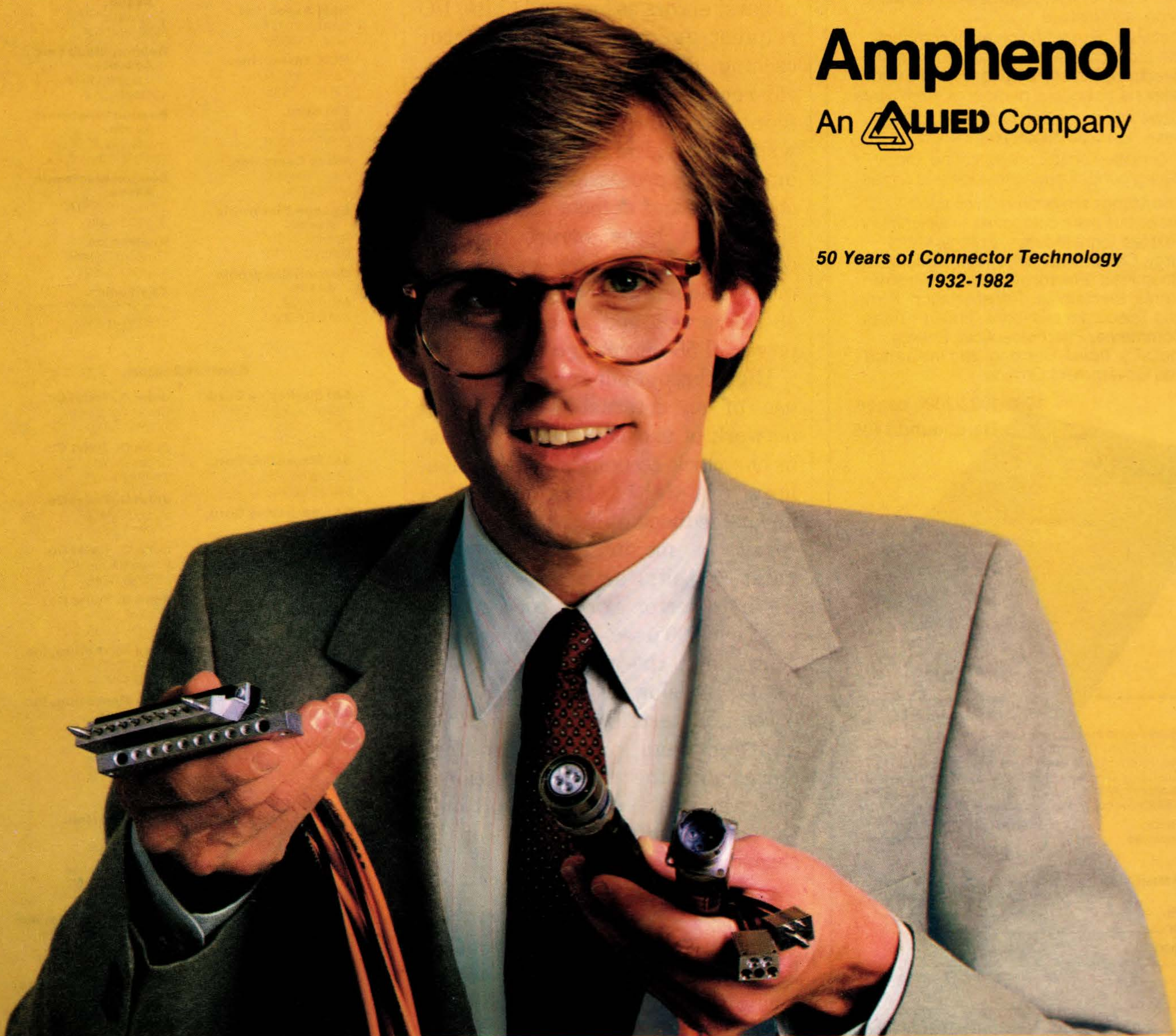
The 7261 also provides internal address-mark detection and ID verification. An 8-bit FIFO aids in loading command parameters and obtaining command results, making the structuring of software drivers

Floppy-disk controllers point the way

Many of the capabilities of the new hard-disk controller ICs have evolved from those available in the more mature floppy-disk controllers. In that arena, most IC manufacturers' products, although termed single-chip devices, still require a few glue parts.

For instance, the NEC 765, Intel 8272 and Western Digital/Standard Microsystems (SMC) 179X Series require clock-regeneration logic, precompensation and buffering to complete the interface. The clock-regeneration logic is available in a single-chip device as the Western Digital 1691 or SMC 9216. SMC will also soon sample the 9229, which integrates clock regeneration, precompensation and buffering into a single chip. And Western Digital has integrated into one chip everything required to interface a floppy except a trimmer potentiometer. Several versions of the chip are available as the WD279X Series.

Also appearing in the floppy-disk arena are IC controllers for the Sony 3½-in. floppy-disk drive. This drive requires a controller different from that for a 5¼- or 8-in. unit because it uses less filler between records and thereby gains more efficient use of disk space. NEC offers the 7265 controller for the Sony drive; because no standard has yet appeared for microfloppy drives, other chips have not yet appeared.



a simple task. The FIFO also serves to buffer data during DMA read/write operations.

Fast bipolar controller

Advanced Micro Devices has also introduced a hard-disk controller IC. This bipolar Am29116, designed specifically for applications such as disk control, can combine with the Am9520 burst-error processor to form a disk controller with bandwidth greater than 20 MHz.

The controller can furnish such features as detection and correction of burst errors as long as 11 bits, I/O request-queue sorting, sector caching, device transparency, logical-record I/O, and associative (content-addressed) reading and writing of logical records. With the burst-error processor, it generates check bits and detects and corrects single and burst errors for four different modified Fire-code polynomials—including the widely used 48-bit version and an exceptionally powerful 56-bit configuration.

High throughput results from the use of an internal 8-bit parallel network of exclusive-OR gates that in one clock accomplish the equivalent of eight clockings of a linear-feedback shift register. As a result, a maximum-length error burst (11 bits) anywhere within a 256-byte sector can be corrected in less than 200 μsec. (With most other controllers, the speed of computation is so slow that when a read error is detected, it's faster to try another read operation before performing the error correction—that way, if the error is a soft one, the data can be read correctly on the second try.)

Improved data integrity

National Semiconductor's entry in the hard-disk-controller arena is a 4-chip set consisting of the DP8460 data separator, DP8462 MFM data encoder, DP8464 disk-pulse detector and DP8466 disk-data controller. These circuits operate at data rates to 25M bps and interface to

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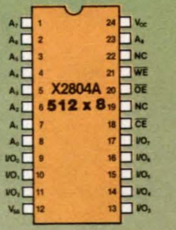

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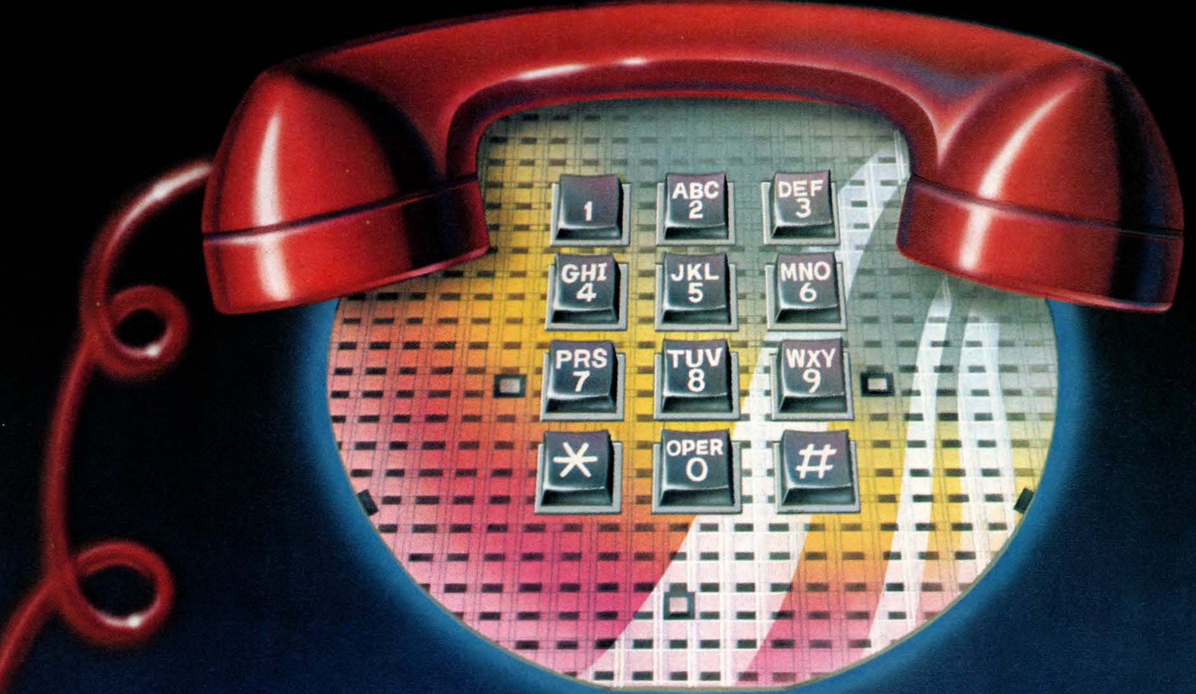

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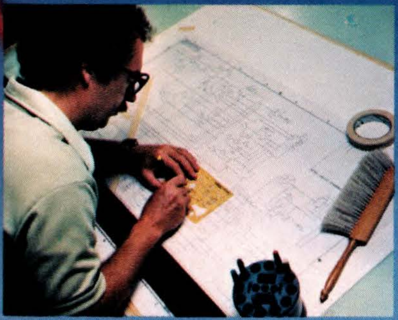

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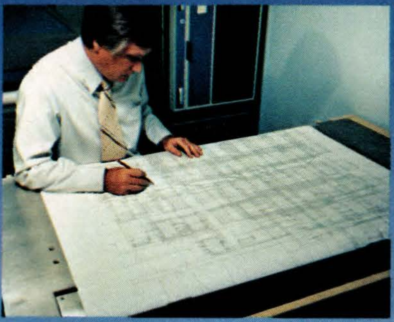

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ST506-, ANSI- or SMD-type drives.

The data separator converts raw MFM input data from the disk-pulse detector into NRZ data and a corresponding read clock that can go directly to the disk-data controller. The heart of this chip, a phase-locked loop, quickly locks onto the incoming data and remains locked in order to produce the stable, glitch-free read clock. If the disk uses run-length-limited code rather than MFM, a synchronized output accommodates external conversion to NRZ.

The MFM data encoder translates serial NRZ data from the disk-data controller into the MFM code that gets written to the disk-head amplifier. In soft-sectored drives, it generates a missing clock with the address mark. Precompensation is also provided; depending on the input data pattern, it can be early, nominal or late by an amount programmable between 0 and 20 nsec.

The disk-pulse detector converts the analog signal from the head preamplifier into digital pulses. It accommodates various recording schemes, including MFM and run-length-limited codes. This chip includes an input amplifier with automatic gain control, a peak detector, an on-chip delay line, an amplitude discriminator and pulse-width-generation circuitry. Its output provides TTL-compatible pulses that correspond to the flux changes (to the data separator) recorded on the disk.

The disk-data controller locates the selected disk header and then converts serial data to 8- or 16-bit parallel data (during read operations) and parallel data to serial data (during write operations). This circuit is also responsible for generating the preamble, address-mark, sync, header and postamble patterns, all externally programmed.

An internally generated cyclic redundancy code (CRC) and 4-byte Fire code are provided, along with hooks for external ECC. DMA

For more information...

For more information on the hard- and floppy-disk controllers described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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Technology

capability is also provided, and an internal 16-word FIFO buffers incoming and outgoing data, removing critical system-timing constraints. The disk-data controller interfaces to the data separator and MFM data encoder on the disk side and the local bus on the system side.

A host of solutions

A final hard-disk-controller option comes from Western Digital, which offers a broad line of hard-disk controllers at both the chip and board levels. The $37.50 (OEM qty) WD1100, available since 1980, comes as a 5-chip set and also as the $295 (OEM qty) WD1000 board-level product. Adding ECC capability increases the number of chips to seven; the resulting set is numbered WD1101, and the equivalent board product is the WD1001.

Western Digital will soon sample single-chip controllers. The WD1050, designed for SMD drives, will furnish an 8-macro-command set for read/write and control functions, a 16-bit data bus, DMA capability and a 10M-bps data rate. A 5-word, 10-bit register will serve as a task file and provide parameter information to process a selected command. The controller/formatter will also provide a handshake signal for external ECC compatibility. Western Digital will also offer the WD1010 controller chip, which will provide a floppy-disk-like interface for ST506-type drives. **EDN**

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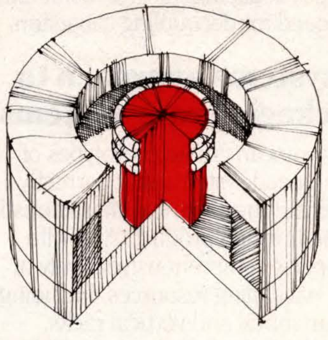

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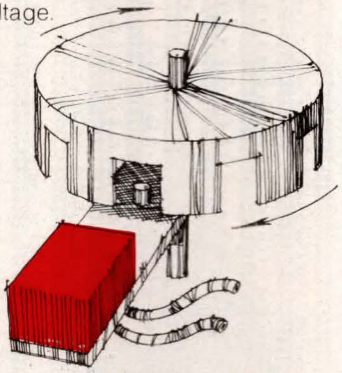

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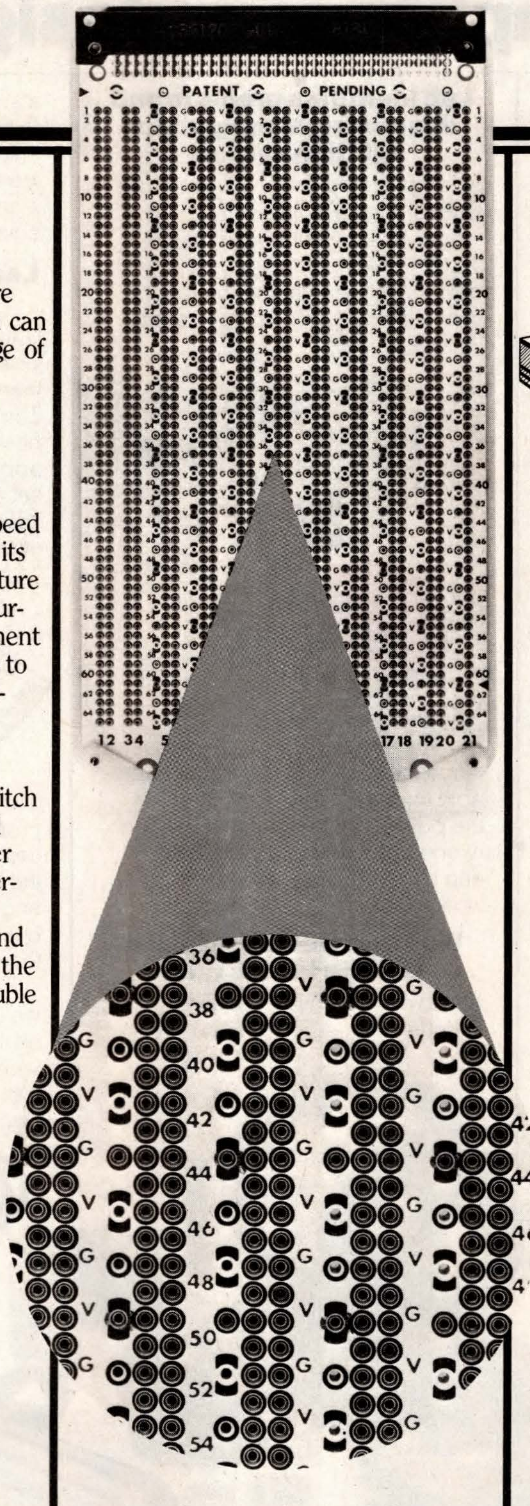

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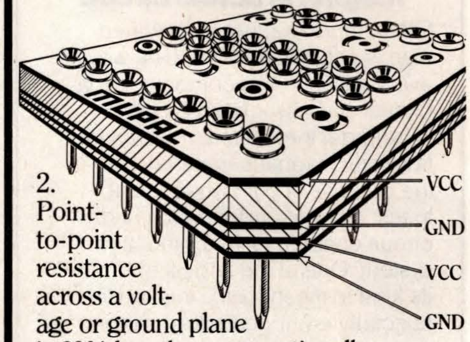

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EDN Semicustom-IC Design Series

Semicustom-logic suppliers differ on how to best deal with testability

William Twaddell, Western Editor

Although suppliers of semicustom logic acknowledge the importance of designing for testability, they've as yet reached no consensus on how to best encourage their customers to do so. All agree, though, that as the use of complex semicustom structures with more than 1000 gates becomes more commonplace, simulation-based testing methods will prove less fruitful than they now do with less complex devices: It will be harder to design products that remain error free in the field. Newer testability-analysis software packages will help ease the testing burden, but some form of built-in self-test appears to be the long-term solution.

Engineers learn to test

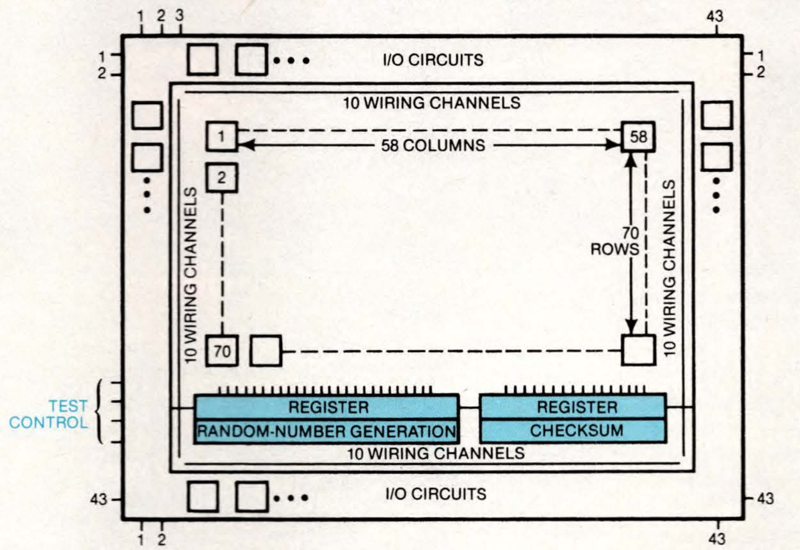
In its early years, semicustom logic (and gate-array technology in particular) was all hand drawn and checked. Gate count stood in the low hundreds, and testability wasn't a problem; manufacturers' primary job was to convince customers that they needed gate arrays at all. That battle is for the most part over, although customer sophistication in dealing with semicustom logic is still limited.

But a problem remains as manufacturers attempt to encourage users to incorporate testability into their semicustom products: In addition to increasing their design sophistication, the users must assume new design functions. Traditionally, the testing chore has rarely fallen to the design engineer, and even more rarely has it been the province of the systems engineer who is most often involved in semicustom-device design.

According to Mohammed Meraj, product-engineering manager for gate-array products at American Microsystems (Santa Clara, CA), most designers have a budget for die size, cost, number of pins and time to production before they start to work on a chip. Convincing them to take a little more time and give up some chip area and pins for testability purposes is not easy. In addition, the firm's Dr R Chandramouli, staff engineer for design automation systems, notes that no numbers yet exist to quantify the benefits of designing for testability, making the job all the more difficult. AMI, like most suppliers, is searching for the structures that give the greatest boost to testability with the least impact on cost.

The criterion for effective incorporation of testability features at California Devices (San Jose, CA) is a die-size penalty smaller than 10%, says vice president for engineering Larry Roffelsen. CDI is designing testability features into its next-generation gate-array product, but Roffelsen says that the lack of a generalized method is making the effort a slow one.

Like Roffelsen, Semi Processes (Santa Clara, CA) consultant (and industry old-timer) Charlie Allen decries the lack of a general method of designing-in testability. But he has a different solution. Because the probability of an error reaching the field increases with the size of an array, his firm keeps array size smaller than about 300 gates. This approach allows SPI to become involved in the design of the final product, so it can help a customer



First of the large arrays *to include an on-chip test facility that's defined by the supplier and serves a maintainability function, National Semiconductor's SLX 6360 packs 6000 gates of 3-μm silicon-gate dual-layer-metal CMOS into a 172-pin-grid package. Its internal pseudorandom-number generator can produce 189-bit vectors at rates to 20M vectors/sec.*

with any testability problems that might arise. In support of this viewpoint, Allen contends that almost all gate arrays designers might contemplate will have fewer than 1000 gates anyway.

Of course, the companies developing larger-gate-count products hold a somewhat different view. But they do agree with Allen regarding the difficulties involved in testing complex logic products. For instance, although Fujitsu encourages its customers to design-in testability, it has no way of checking their efforts because it can't get involved in the actual chip design. It does, however, provide software that as part of a design's simulation can estimate the number of nodes that toggle.

Moreover, the logic-simulation process is itself somewhat useful for testability purposes; it allows a user to generate a set of test vectors that functionally exercise a completed array. The simulator exercises all nodes with a specified input pattern; the software then examines any logic races and hazards that exist. Supplemental programs can enumerate the percentage of gates exercised and estimate fault coverage. In addition, stuck-at-ONE/ stuck-at-ZERO fault-grading programs analyze input-vector efficiency by sequentially holding every node at a ONE or ZERO.

Indeed, simulators such as TEGAS and LOGCAP are widely used as gate-array designers' primary tools. For this reason, a good simulator is a good selling point—a fact not lost on ZyMOS (Sunnyvale, CA) when it designed its ZyPSIM. It functions only with the company's standard-cell design system and interfaces to Fairchild Sentry VII or System 20 testers.

Bill Loesch, director of marketing and sales, notes that a semicustom-logic supplier can build greater sophistication into a simulator aimed at a specific design system. For instance, ZyPSIM won't allow a blanket reset of all gates as some other simulators do. Rather, it decides if an initialization is physically performable before allowing it to proceed.

In addition, because it only works on ZyMOS standard cells, the simulator provides an accurate timing simulation of a silicon implementation. As a result, it can produce the actual test time of the generated test vectors. It can also detect cycle slipping, in which varying logic speed causes an output change around the tester strobe point.

Testability analysis needed

As sophisticated as some simulators are, however, their fault-grading programs are not sufficient to ensure a design's testability; simulation focuses primarily on design feasibility. Tools for testability evaluation are being developed, though; termed testability-analysis programs, most derive from the Sandia Controllability/Observability Analysis Program (SCOAP) developed at Sandia National Laboratories (Albuquerque, NM).

In Sandia's definition, designing for testability involves providing readily accessible control and observation paths to all functional units within a device. The SCOAP software thus calculates six functions that characterize the controllability and observability properties of a digital network. In this context, controllability measures the degree to which the internal nodes' logic states can be controlled from the primary inputs, and observability measures the degree to which the nodes' logic states can be discerned at the primary outputs.

Several analysis programs based on SCOAP are used in in-house programs at various manufacturers. They include TICOP at Texas Instruments (Houston), CAMELOT at Cirrus Computers (United Kingdom) and COMET at United Technologies Microelectronics Center (Colorado Springs, CO).

The COMET program (Controllability and Observability MEasure for Test) is especially interesting. It generates a number score for each node in each of the six testability areas; based on the relative ranking of these numbers, a designer can determine the technique to use to correct a test problem.

For instance, a very high number in the controllability or observability function for either sequential or combinatorial logic indicates the need for a test point. And because COMET is an interactive program, it can insert specified test points and determine their effect on the testability of both a node and the circuit as a whole. If the added test points prove insufficient, the designer can add more—singly or in groups. The program also generates a statistics file that provides averages for controllability, observability and testability of combinatorial and sequential circuits. With this aid, the designer can easily spot nodes that are out of bounds.

COMET can be run any time after logic interconnections have been described. Because it can't uncover every possible testing problem, it's usually run in conjunction with a simulation program.

Ad hoc or structured approach?

Even in conjunction with a simulation program, though, testability analysis can only tell that a design needs modification to improve testability; the modification itself is up to the designer. But how do you proceed? Robert Rozeboom of Texas Instruments's Design Automation Group explains that three methodologies are now in use: ad hoc and structured techniques and built-in test.

The ad hoc method is the one used by most manufacturers concerned with testability to any degree. For instance, United Technologies supplies a testability handbook as well as the COMET software, giving a laundry list of testability techniques from which you can choose. These techniques include using flip flops with their Clear pins tied to Reset, partitioning a system into multiple arrays, giving preference to certain cell types and breaking up long counter chains.

The structured methodology is practiced primarily at large companies with in-house fabrication or design capabilities. The most widely discussed technique is IBM's level-sensitive scan detection (LSSD), but others exist at companies such as NEC, Hitachi, Siemens and Sperry. Using shift registers and serial techniques, LSSD reduces the testing of sequential logic into the more easily tested combinatorial case. Problems cited for this method, however, include limits on circuit performance, lack of testing at functional operating rates and on structures such as embedded RAM, and serial shift sequences several hundred times slower than those accomplished with parallel access. Detractors also note that testing an LSSD-designed chip is a different process at wafer test than at final test and—worst of all—impossible to enforce on customer/designers in any event.

Bill Berg, project manager for testability design at United Technologies, addresses the problem of enforcement by noting that designers must be philosophically convinced of the need for designing-in testability; forcing a costly (5 to 25% die-area penalty) structured method on them won't work. Berg thinks education and ad hoc techniques will provide the best method of introducing testability issues to designers.

TI's Rozeboom concurs with Berg on the need for education. And he adds that TI tries to sensitize its customers to an approach that reduces product life-cycle costs. The firm also stresses an understanding of the equation already well understood by semiconductor manufacturers: The cost of finding a problem increases by an order of magnitude at each step in a product's development cycle.

One of TI's methods of easing the testing burden is what it terms bus-oriented design—a technique in which the designer partitions the logic into pieces connected by a bus that also connects to the device's external pins. Control information shifted onto the bus can then enable or disable blocks of logic for testing.

Another TI technique, used in the firm's TMS 1000 single-chip-μC program, is applicable to any ROM-programmable product. In this case, the customer includes in his microcode a set of instructions that allow the testing of blocks of the μC. These same instructions can be used when the μC is executing a program.

Other manufacturers use other built-in test methods. LSI Logic (Milpitas, CA), for example, offers a form of scan detection that requires three pins and 10 to 20% more gates. And California Devices is investigating a RAM-like structure that can read and write to nodes but also serve other purposes if not used for providing testability.

The latter firm's Roffelsen notes that most gate-array manufacturers would like to include hardware to enhance testability in their products. But they want a method that incurs no penalties—a tough requirement to satisfy.

For instance, Motorola (Mesa, AZ) includes a diagnostic and chip-control section in its Macrologic arrays. The section doesn't limit functionality or performance, but it does tie up three I/O pins and consists of 500 I^2L gates. This added logic can monitor the status of 48 internal test points, load test or program data into an 8-bit latch that feeds into the 48 test points, and generate reset or clock signals to verify circuit operation.

An even more sophisticated technique, used by National Semiconductor (Santa Clara, CA), adds not only testability but maintainability. The penalty here, though, is the use of about 15% of the die area of a 6000-gate array.

The concept, named BILBO (Built-In Logic Block Observation) employs on-chip hardware that includes a 189-bit polynomial pseudorandom-number generator that can be seeded externally. Feeding into a device's input pins in parallel, the generator can achieve a speed of 20M vectors/sec. As these vectors filter through the circuit, they get collected by an 88-bit checksum register connected to the output pins. As each resultant enters the register, it gets added to the previous resultant; after a very large string of input vectors propagates through, the final resultants get summed to form an 88-bit signature that should be identical for all parts tested with the same seed vector. Because all the logic is on chip and controlled from four test pins to the package, testing can occur in the field and the factory.

This parallel-signature-analysis technique can isolate problems in addition to providing Go/No-Go testing. For example, equipotential nodes can be mapped by means of the checksum register's contents. National believes the technique is capable of generating 100% controllability/observability, but at this stage it's willing to settle for 80% fault coverage at a reasonable price. **EDN**

References

1. Albrow, R, and Robinson, G, "VLSI CAT: Filling the void between CAD and testing," *VLSI Design,* September/October 1982, pg 20.
2. Hess, R, "Testability analysis: An alternative to structured design for testability," *VLSI Design,* March/April 1982, pg 22.

Article Interest Quotient
(Circle One)
***High* 506 *Medium* 507 *Low* 508**

1982 IEDM to continue transition toward practical coverage

John Tsantes, Eastern Editor

The 28th annual International Electron Devices Meeting (IEDM), slated for December 13 to 15, marks a departure from its predecessors in both technical content and location. With its move from Washington, DC to San Francisco, the show takes a symbolic step closer to the industry it covers. And with that step, it continues to place greater emphasis on practical developments.

The 3-day meeting will feature 188 technical papers, divided among 31 sessions on such topics as solid-state devices, device technology, integrated circuits, electron tubes, quantum-electronic and energy-conversion devices, and detectors, sensors and displays. Because of the technical program's increasing emphasis on next-generation products rather than long-term development projects, a greater number of EDN's readers are likely to find this IEDM more immediately useful than previous ones.

Advanced µPs

A variety of interesting developments will be discussed in all six major session groupings (see **box,** "IEDM highlights and schedule"). For instance, in one session, researchers from Bell Telephone Labs will report on enhancements to Bell's twin-tub CMOS process. These enhancements have yielded a 150,000-transistor, 32-bit microprocessor chip; the advanced process, using 2.5-µm design rules, is also being applied to a 4-bit microcomputer family as well as to static memories.

In another presentation, General Electric representatives will discuss a new gate-turn-off (GTO) power device, termed the insulated-gate rectifier. This device, which combines the high input impedance of an MOS gate with the high operating-current density of bipolar devices, specs breakdown voltage of 650V and 20-µsec switching time.

Speed improvements

If you're interested in fast RAMs, take note of Mitsubishi's talk, scheduled for a subsequent session. The company has reportedly built one of the fastest 64k dynamic RAMs available: It specs access time of just 55 nsec. The device employs a triple-diffused-junction MOS process.

Developments in even faster gallium-arsenide devices will be covered in another IEDM session. There, a Bell Labs paper will review the fabrication of an 11-stage, directly coupled, selectively doped heterojunction-transistor ring oscillator that exhibits a sub-20-psec propagation delay.

Thomson-CSF presenters will also focus on high-speed operation in a paper on GaAs/AlGaAs 2-dimensional electron-gas FETs (TEGFETs). The process used to fabricate these devices requires no recessed or self-aligned gates, as do

		CONTINENTAL BALLROOM 1,2,3	CONTINENTAL BALLROOM 4	CONTINENTAL BALLROOM 5
MONDAY DECEMBER 13	9:00 AM 11:45 AM			PLENARY SESSION (Invited Papers)
	1:00 PM 4:30 PM	ELECTRON TUBES—TRAVELING-WAVE TUBES 2	DEVICE TECHNOLOGY—INSULATORS AND ISOLATION 3	
	6:00 PM 7:00 PM			WINE AND CHEESE RECEPTION
TUESDAY DECEMBER 14	9:00 AM 12:00 PM	ELECTRON TUBES—MICROWAVE-TUBE THEORY 8	DEVICE TECHNOLOGY—MOS DEVICE ISOLATION 9	
	12:15 PM 2:00 PM			
	2:15 PM 5.30 PM	ELECTRON TUBES—GYROTRONS AND GYRO-TWTs 14	DEVICE TECHNOLOGY—LITHOGRAPHY AND PATTERN TRANSFER 15	
	8:00 PM 10:00 PM	PANEL DISCUSSION—THE SILICON FOUNDRY—MYTH OR REALITY? 20		PANEL DISCUSSION—HIGH-VOLTAGE INTEGRATED CIRCUITS 21
WEDNESDAY DECEMBER 15	9:00 AM 12:00 PM		DEVICE TECHNOLOGY—ADVANCED INTERCONNECT TECHNOLOGIES 24	
	1:30 PM 5:00 PM		DEVICE TECHNOLOGY—ADVANCED MOS TECHNOLOGIES 29	

conventional GaAs FET devices. Thus, the firm says it will ultimately produce parts with delay times of 10 psec and 1-μm gate lengths.

In this same session, NEC will report on a 0.3-μm-gate-length super-low-noise GaAs MESFET. The firm will discuss the unit's 0.3- to 0.5-dB (4 GHz) and 1.2- to 1.4-dB (12 GHz) noise figure—especially noteworthy because the device is manufactured on a volume-production basis.

Fujitsu's developments in the area of isolation technology for high-speed, high-density bipolar memories will be outlined in another IEDM paper. The firm's IOP-II (isolation with oxide and polysilicon) process uses a deep silicon U-groove for isolation. With it, Fujitsu has developed a 16k RAM with 15-nsec access time and 750-μm^2 memory-cell size.

Sensitive transistors

One of IEDM's more interesting

IEDM highlights and schedule

The 1982 IEDM will be held in the San Francisco Hilton and Tower Hotel. Its 31 sessions will be organized in six broad categories:

Device technology—New developments in materials and processing technology (eg, thin dielectrics, device isolation, beam annealing, interconnects for wiring and personalization; pattern transfer and lithography) will be featured. Emerging device technologies in CMOS/NMOS and silicon-on-insulator environments will be covered in two sessions.

Solid-state devices—Highlights this year will include 1000V ICs, 200-MHz MOS power transistors, high-voltage silicon switching devices, high-yield GaAs ICs, novel silicon permeable-base transistors and short-channel FETs.

Integrated electronics—Gigahertz-speed CMOS circuits and latchup-free structures, 55-nsec 64k dynamic RAMs and nonvolatile RAMs with dynamic-RAM densities, 290-psec I^2L processes with fivefold self alignment, and scaled devices will all be covered.

Electron tubes—Advances in electron-tube design, including millimetre-wave and gyrotron devices, are some of the highlights here. Theory and fabrication of RF-interaction circuits, electron guns and cathode technology will be emphasized.

Quantum electronics—Components for fiber-optic communications and optical recording, fast detectors, and high-performance laser devices will be a few of the topics in this category.

Detectors, sensors and displays—Look for treatment of advances in device theory, performance, modeling and processing, plus integration of solid-state photodetectors; advances in solid-state sensors and transducers for environmental, biomedical and control applications (with emphasis on integration of the sensors with other circuit functions); and advances in display devices.

CONTINENTAL BALLROOM 6	CONTINENTAL BALLROOM 7,8,9	IMPERIAL BALLROOM	HILTON PLAZA	PACIFIC ROOM	FRANCISCAN ROOM
	1				
SOLID-STATE DEVICES—HIGH-VOLTAGE INTEGRATED CIRCUITS 4		INTEGRATED CIRCUITS—ADVANCED INTEGRATED STRUCTURES 5	DETECTORS, SENSORS AND DISPLAYS—INFRARED DETECTORS AND MATERIALS 6	SOLID-STATE DEVICES—III-V DEVICE AND CIRCUIT TECHNOLOGY 7	
SOLID-STATE DEVICES—HIGH-VOLTAGE DEVICES AND POWER FETs 10		INTEGRATED CIRCUITS—MODELING 11	DETECTORS, SENSORS AND DISPLAYS—SILICON SENSORS AND DISPLAYS 12		QUANTUM ELECTRONICS—III-V HETEROSTRUCTURE PHOTONIC DEVICES 13
				IEDM LUNCHEON	
DEVICE TECHNOLOGY—TECHNOLOGIES FOR SILICON-ON-INSULATOR DEVICES 16		INTEGRATED CIRCUITS—SCALED CMOS 17	SOLID-STATE DEVICES—DISCRETE AND MONOLITHIC BIPOLAR DEVICES 18		QUANTUM ELECTRONICS—PHOTOVOLTAIC AND PHOTOCONDUCTOR DEVICES 19
PANEL DISCUSSION—HIGH-SPEED DEVICES AND TECHNOLOGY 22		PANEL SESSION—BIPOLAR AND MOS TECHNOLOGY—CHOICES FOR VLSI APPLICATIONS 23			
SOLID-STATE DEVICES—HIGH-SPEED III-V DEVICES 25		INTEGRATED CIRCUITS—RANDOM-ACCESS MEMORY 26	SOLID-STATE DEVICES SILICON FIELD-EFFECT DEVICES 27	INTEGRATED CIRCUITS—BIPOLAR DEVICES AND MODELING 28	
		INTEGRATED CIRCUITS—NONVOLATILE MEMORY: DEVICES AND MODELING 30	SOLID-STATE DEVICES—NOVEL DEVICES AND TECHNOLOGIES 31		

papers will deal with magnetic transistors. Coauthored by researchers at IBM and North Carolina State University, it will be presented in a session on detectors, sensors and displays.

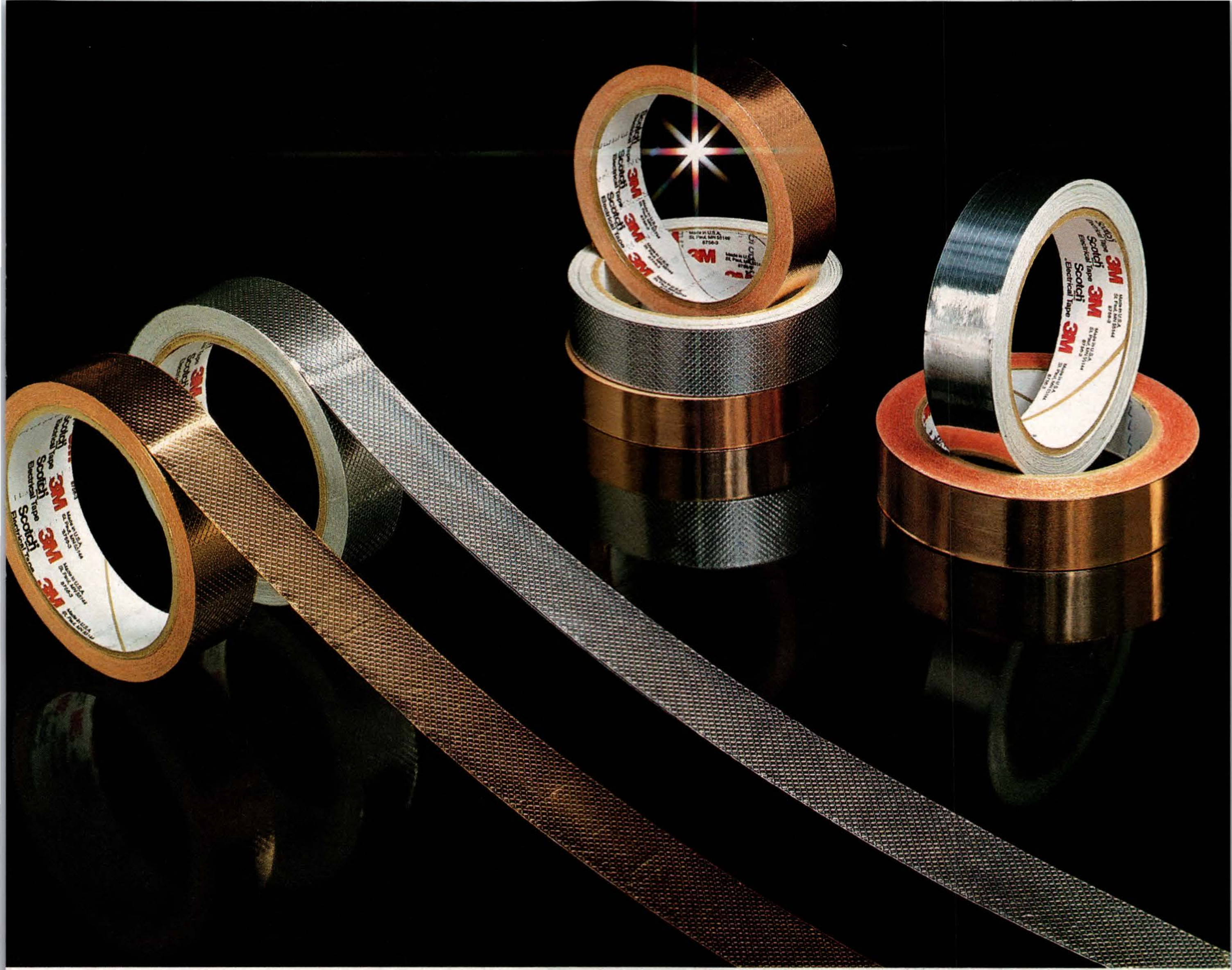
The jointly developed bipolar magnetic transistors are approximately 1000 times as sensitive as Hall cells. They could eventually find wide use in tape/disk read heads, strain gauges and gaussmeters, replacing existing Hall devices, thin-film magnetoresistive elements and magnetodiodes.

The researchers will describe 6-μm-emitter devices operating at 20-mA emitter currents. These parts feature sensitivity greater than 20V/tesla and signal-to-noise ratio of 10^5/tesla for 6-kΩ loads.

During this same session, Toshiba will report on a 3648-element CCD image sensor that can read an 8½-in. page with 16-element/mm resolution at a 20-MHz data rate. The sensor's 1.1×31-mm chip size results from employing 8×8-μm photodiodes and a 3-level polysilicon electrode structure.

There'll be much more to see at IEDM than the foregoing brief outline touches upon. For additional information on the program and for registration material, contact conference manager Melissa Widerkehr at Courtesy Associates Inc, 1629 K St NW, Suite 700, Washington, DC 20006; phone (202) 296-8100. **EDN**

Article Interest Quotient
(Circle One)
***High* 509 *Medium* 510 *Low* 511**



How to foil the high cost of EMI/RFI shielding

Use 3M conductive foil tape. It's an effective, fast way to keep the FCC from giving you static, often at less cost than other shielding methods.

For computer equipment, CATV and other electronic products, 3M copper or aluminum foil tapes are a cost-efficient alternative to conductive sprays, gaskets, plastics, formed metal shields, pastes or product redesign.

3M foil tapes make application and removal fast, clean and easy. The tape is quickly applied only to the areas needed, with no waste, no messy overspray and no special skill or expensive equipment required. Environmentally safe 3M foil tapes eliminate the high energy costs of spraying and ventilation. You can forego contract plating, painting, soldering and cleanup, while improving in-house quality control and turnaround time.

Foil tapes from 3M are durable. They adhere better than many spray films, which can easily scratch, limiting shielding effectiveness, or flake, shorting components. 3M offers embossed tapes that enhance conductivity between foil backing and substrate, and the smooth foil tapes are available with or without our conductive adhesive.

So for easy, time-saving, cost-effective shielding and static control that last, stick with the biggest name in conductive foil tapes: 3M. Specify copper or aluminum foil tape, smooth or embossed, conductive or nonconductive adhesive. For more information, write Industrial Electrical Products Division/3M, 3M Center, St. Paul, Minnesota 55144

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CIRCLE NO 38

low-power design success CMOS M146805 Family.

The list of M146805 features is long. It's hard to know where to start and which to mention. Flexibility derived from a choice among several MCUs is very important. Two ROM versions, 1K and 2K, plus an expandable-bus MPU are available now. A CMOS PIA and Real-Time Clock also are available, and all five devices offer the option of leadless chip-carrier packaging.

Family processors have master and power-on reset, on-chip oscillators, programmable timers with prescaler, maskable interrupts, ten addressing modes, single-instruction bit manipulation and nested subroutines.

		MC146805E2	MC146805F2	MC146805G2
TECHNOLOGY		CMOS		
PROCESSOR	Bits	8 Bits		
	Instruction Set	Control Optimization of MC6800		
	Registers	2 General Purpose and 3 Special Registers		
	Addressing Mode	10 Addressing Modes		
	Basic Inst. Types	61 Basic Inst. Types		
	Total Instructions	209 Total Instructions		
	μs per Avg. Inst.	3.9 to 4.0 μs/Average Instructions (1 MHz)		
	Subroutines	29 Levels	13 Levels	29 Levels
MEMORY	Mask ROM	—	1K	2K
	RAM Bytes	112	64	112
I/O PINS	Inputs	—	4	—
	Program Bidirect	16	16	32
	I/O Drive Capability	LSTTL	LSTTL	16-LSTTL 12-2 mA, 4-LED
PACKAGE SIZE		40 Pin	28 Pin	40 Pin
EXPANSION BUS		8K Addr.	—	—
SPECIAL FUNCTION I/O	High Current Drive	10 mA, 4 Pins	—	—
	Serial I/O	Shift Register I/O with Bit Manipulation Instructions		
TIMER	Prescale Bits	7 Prescaler Bits		
	Counter Bits	8-Bit Counter		
	Timer Functions	One Timer Function at a Time		
INTERRUPTS	Timer Interrupts		Timer Interrupt	
	External IRQ	1	1	1
DEVELOPMENT SUPPORT	IC's	EPROM and ROM-less Versions		
	Dev. System	EXORset™, EXORciser® and Emulator Modules		
	Emulation	User System Emulator		
	Assembler	Macro Assembler		
SPECIAL CAPABILITIES	Self-Check	—	Yes	Yes
	External Bus	Yes	—	—
POWER REQUIREMENTS	Full Spd. Oper.	35 mW	10 mW	15 mW
	Wait Mode	5 mW	4 mW	4 mW
	Stop Mode	25 μW	25 μW	25 μW

M146805 emulators provide tailored CMOS development tools for every processor in the family, and the CMOS M146805 Family software is HMOS compatible. Family peripherals are HMOS compatible too.

Value, finally, is the bottom line, and we don't believe there is a design option that will give you better, more cost-effective value. Motorola's CMOS quality and reliability have been recognized around the world for years, and M6800-type architecture has been widely praised. RCA is now an alternate source for the M146805 Family.

Peripherals add value.

Additional value is provided by a pair of multiplexed-bus peripherals and the MCM1465516 2K x 8 mask-programmable CMOS ROM.

The MC146818 Real-Time Clock is a complete time-of-day clock with alarm and one-hundred year calendar, plus a programmable interrupt and square-wave generator. It has 50 bytes of low-power static RAM on-chip, and interfaces with 1 MHz processor buses.

Twenty-four I/O pins of the MC146823 Parallel Interface are organized into three bidirectional ports. It includes complete control handshake, output pulse, four interrupt inputs and 16 registers addressed as memory locations.

Both of these peripherals have Motorola's unique MOTEL circuitry for interface with M146805 Family processors and most other CMOS and NMOS multiplexed-bus MPUs.

Check off the advantages and send for additional information to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036. Contact your Motorola Sales Office or authorized distributor for fast action in helping you design

Innovative systems
through silicon.

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120 EDN 11/24/82

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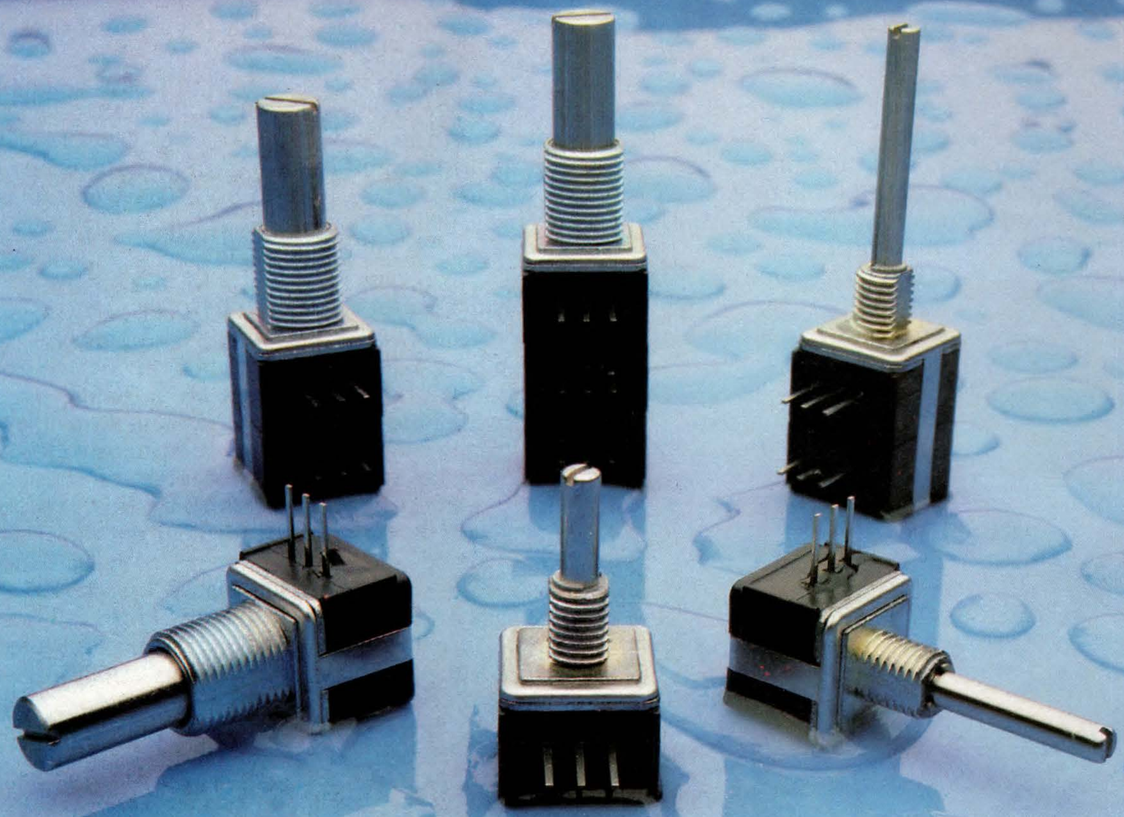
First 1/2" panel control pot...



With a Sealed Option for Board Washing

Now with Spectrol's new Panel Control Potentiometers there's no need to fear board washing. These low-cost 1/2-inch-square units are available in sealed versions to permit cleaning in common solvents. They are also available with various other options including multiple cups, switch sections, special bushings and shafts. The conductive plastic model 148 has a standard resistance range from 100 Ω to 1 megohm, and the cermet model 149 has a standard resistance range from 100 Ω to 5 megohms. With either unit, you get quality performance and competitive pricing. For full information, send for a data sheet today.

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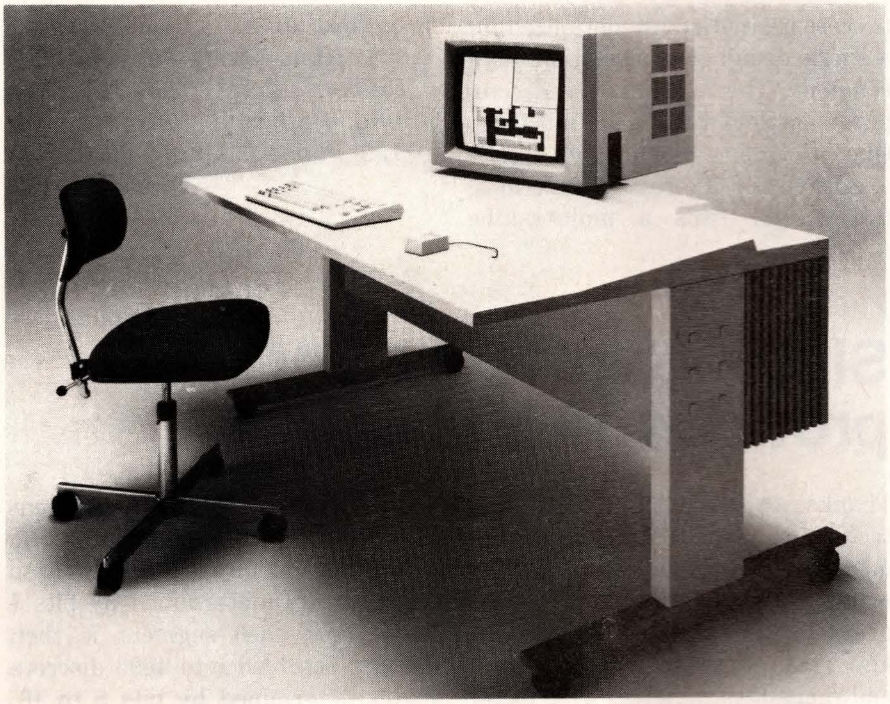
CIRCLE NO 39

Integrated engineering workstation speeds VLSI-circuit design

By supporting schematic-entry, circuit-simulation and IC-layout tasks, the λ750 CAE system epitomizes the trend toward the totally integrated engineering workstation. It allows one engineer to perform all the steps involved in system and VLSI design—from initial conception through schematic generation, physical layout, performance verification and project documentation. Moreover, by providing a common set of tools for all engineers involved in product development, the workstation also enhances design-team communication, productivity and creativity. (For further discussion of integrated engineering workstations, see EDN, October 14, 1981, pg 248; March 31, pg 41; and July 16, pg 106.)

What separates the $75,000 λ750 from previously introduced CAE workstations is its ability to function as a complete color CAD system as well as support logic-design tasks. The single-user system employs an enhanced version of its manufacturer's Ω400 color-graphics processor to provide 1024×768-pixel, 512-color resolution on a 19-in. monitor. Sixteen display-memory planes facilitate hierarchical, nested physical-layout operations, and the graphics processor's integral 68000-μP controller accommodates vector drawing at rates to 1 million pixels/sec and polygon fills at speeds as high as 16 million pixels/sec.

The λ750's interactive layout editor fully exploits the graphics system's speed and resolution, supporting geometric IC-mask development as well as symbolic cell-placement and -wiring operations. It also displays multiple windows for simultaneous viewing of foreground and background functions.



Supporting physical layout *as well as logic-design-simulation and -documentation tasks, the λ750 CAE workstation provides high-resolution color graphics. It furnishes all the features of a conventional CAD system and includes tools for standard-cell placement, gate-array interconnection and PLA generation.*

Workstation physical-layout capabilities become increasingly important as more system designers undertake IC-development projects. Many producers of gate-array and standard-cell design software claim that their systems offer complete layout capability without the need for high-resolution, CAD-like color graphics. Most design efforts, however, require some manual interconnection routing or cell customization. Furthermore, says company president Gene Chao, engineers generally want to be aware of all phases of design activity, including functions that automated tools perform. Thus, designers require an ability to view, analyze and modify the layouts that software programs generate.

By allowing designers to transfer graphical data to and from other design systems, the λ750 enhances designer communications. Using a CIF (Caltech Intermediate Format) database exchange, operators can monitor work done with the aid of other CAD systems—including pc-board- and mechanical-design workstations. This capability helps design-team members optimize their efforts.

Speed design cycles

An optimized CAE workstation must integrate hardware and software system-design capability to permit engineers to achieve maximum productivity. Designer productivity represents an especially critical concern in VLSI development projects involving large, complex and nonrepetitious chips. Director of VLSI engineering

Chong Lee says that the lack of sophisticated, integrated IC-design tools has contributed to the significant device-density differences between memory chips and other device types. Because memory chips typically employ regular arrays of replicated cells, memory design is compatible with automated layout and designers can therefore more readily exploit process-technology advancements. Random-logic circuits, however, require considerable operator intervention during cell design and layout and therefore require slower development cycles.

To simplify and speed IC design tasks, the λ750 includes hierarchical design software that reduces the time required to develop large devices. The programs embody incremental methodologies that take advantage of design regularity to eliminate repeated simulations of previously characterized and unchanged circuit elements. As a result, the system reduces performance-verification times and allows interactive simulations and design-rule checks.

The workstation's standard design software includes a text-processing program for project specification and documentation, schematic-entry routines based on a symbol-creation editor, an event-driven logic simulator, SPICE for circuit simulation, symbolic and geometric layout tools, a circuit extractor that derives electrical data from physical layouts, a net-list comparator that checks extracted circuit data against logic schematics, a post-layout simulator and an electrical-rule checker.

The λ750 also comes with an NMOS standard-cell library composed of approximately 30 basic function blocks such as gates, flip flops and ALUs. The workstation's integral design-rule checker simplifies the generation of mask data suitable for fabrication by multiple vendors by accepting user-defined MOS process specifications; design rules and CMOS cell libraries from several silicon foundries already exist in the λ750 internal format. Moreover, the standard software package includes a PLA generator—a primitive silicon compiler that translates truth tables directly to optimized array-logic mask data.

To support user-generated applications programs and provide database-management capabilities, the λ750 runs under a superset of University of California at Berkeley UNIX. A standard 300-baud autodial modem allows intersystem communication as well as remote diagnostics; other standard interfaces include six RS-232 serial ports, two RS-449 serial channels and an IEEE-488 port. In addition, the λ750 standard software includes a communications routine that allows the workstation to function as a terminal connected to a host processor. An optional single-board Ethernet controller further enhances the system's I/O capability.

Because hardware/software integration proves crucial in tools designed to improve user productivity, the λ750 employs a proprietary processor architecture optimized for a single-designer workstation environment. The Multibus-based computer employs two 12-MHz 68000s. One processor handles all UNIX executive and file-related functions; the second runs a multitasking real-time operating system that controls all memory-management and I/O functions. The λ750 includes 1M bytes of physical RAM (expandable to 4M bytes using 64k-bit devices or 16M bytes with 256k-bit RAMs), and the processor supports demand-paged virtual-memory operations. To maintain a short product-development cycle and ensure optimum packaging density, the workstation's designers used programmable logic arrays extensively. The tools to design a custom-IC based processor didn't exist at the outset of the λ750's development, Lee points out.

The workstation's standard mass-storage devices include a 30M-byte Winchester drive and a 1M-byte 5¼-in. floppy-disk unit. An optional tape drive allows software porting as well as archival data storage.

The λ750 comes packaged as a desk-like station and includes a detachable keyboard, a data-input mouse and a relocatable monitor movable on three axes. To eliminate the need for conditioned power, the workstation includes short-term battery backup that saves work in progress after a 1-min power interruption.—***Andy Rappaport***

Metheus Corp, 5289 NE Elam Young Parkway, Hillsboro, OR 97123. Phone (503) 640-8000.

Circle No 453

Single-chip 16-bit DAC provides 14-bit linearity

Thanks to a novel bit-decoding technique, the HS3160 16-bit 4-quadrant multiplying D/A converter guarantees 14-bit monotonicity over 0 to 70°C. The decoding scheme also reduces sensitivity to switch and resistor parameters by a factor of eight and decreases output capacitance to improve settling time and signed feedthrough.

Segmentation is a key ingredient in the decoding process. The transfer function first divides into 16 segments (determined by bits 1 to 4), and each segment is then further resolved into 4096 discrete levels determined by bits 5 to 16. Bits 1 to 4—digitally decoded into 16 lines—drive equal current sources, not binary-weighted ones.

Are You a Current Battery Expert? Try this Designer's Quiz

Normally, Globe Battery Division is the leader in battery answers. In this case, we'll lead with some questions. See how you fare with this battery quiz.

Question 1—True or False:

When comparing two batteries of identical volumes but with different capacity ratings, the battery with larger capacity is probably a better battery.

Answer:

False. There is no correlation between capacity and quality. However, there is a correlation between capacity, volume and life. The rule of thumb is, the lower the capacity for a specific volume, the longer the life.

Higher capacity (rated AH) is achieved by increasing the amount of lead in the battery. Within a specific volume however, an increase in the amount of lead can only be accomplished by reducing the amount of electrolyte, resulting in premature failure due to recharge problems.

Question 2—True or False:

When testing identically rated batteries, initial capacity is not an accurate gauge of battery quality.

Answer:

True. Initial capacity is not a very good method of judging the quality of a battery. In some cases, manufacturers choose to improve the initial capacity of their batteries by lowering the paste densities. However in so doing, the shedding of plate material substantially decreases its cycle life. (See illustration below)

Globe Gel/Cells are designed for extended cycle life, while optimally meeting initial capacity criteria. Unsurpassed performance over the life of the cell, and extended cycle life is what sets Gel/Cell apart from the rest.

Question 3—True or False:

A "deep cycle" occurs when a battery is rapidly discharged to a very low voltage.

Answer:

False. Depth of discharge (or deep cycle) is determined by the percentage of rated capacity extracted from the battery. A deep discharge occurs when 80%-100% of the capacity is discharged, as in the case of a low current discharge over an extended period of time.

For example, reducing the voltage in an automotive battery to the point where it can't crank the engine is not a deep cycle. In actuality, only approximately 10% of the capacity has been discharged. However in the case of a battery driven wheelchair, where 70%-90% of capacity can be discharged during continued use, deep cycles are recurrent. When specifying batteries for deep cycle applications, be sure to get the percentage of capacity discharged during the tests. At Globe Battery Division, our data on cycle life is always based on minimum discharge depths of 85% of capacity.

Question 4—True or False:

Failure of batteries in float applications is usually caused by loss of electrolyte due to gassing during continuous charging.

Answer:

False. Electrolyte loss due to gassing contributes little to the potential failure mode of batteries in float applications. Actually, grids would corrode long before gassing could have any effect on the life of the cell. Therefore, the thickness of the grids has much more bearing on float life than gassing.

Question 5:

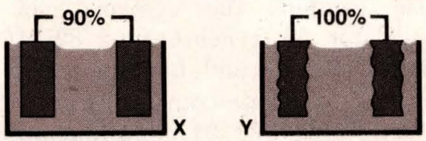
Is there a way for you to get more information on the implications of battery technology on your designs?

Answer:

Absolutely. Globe Battery Division would be pleased to schedule a seminar conducted by our engineers to provide you and your staff with more in-depth information. Information that can help you make better use of battery technology in your designs.

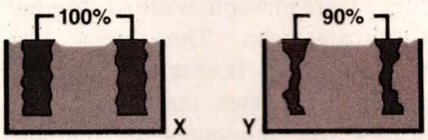
With 70 years of experience in lead acid battery technology, Globe Battery Division has established a tradition of providing knowledgeable assistance to design engineers. Call or write Mr. Robert Scrima at Johnson Controls, Inc., Globe Battery Division, Industrial Products Group, 900 East Keefe Avenue, Milwaukee, WI, 53201, (414) 228-2398.

How initial capacity can affect the cycle life of a battery.



After 1-5 cycles

Battery Y shows a higher initial capacity because more plate surface is exposed to electrolyte—a result of increased irregularities in its surface (low density). However after 100 cycles battery X (high density) meets its rated capacity, while battery Y's capacity has deteriorated due to shedding of plate material. Look beyond initial capacity when testing a battery for your needs.



After 100 cycles

gel/cell®

Globe Battery Division

JOHNSON CONTROLS

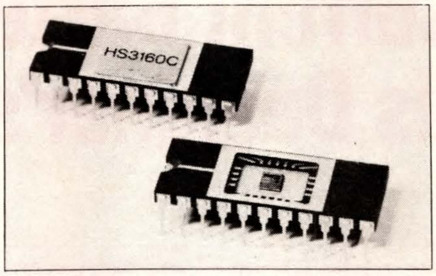
CIRCLE NO 40

Technology Update: New Products

In its unequivocal guarantee of 14-bit monotonicity over temperature and its stand-alone operation, the HS3160 differs from two other major single-chip offerings:

- Intersil's ICL7134, using PROM nonlinearity correction, exhibits 0.003% (14-bit) nonlinearity at 25°C and typical nonlinearity drift of 1 ppm/°C. At 70°C, this causes approximately 0.005% additional nonlinearity, for a total of approximately 0.008%—ie, 12½-bit monotonicity (typical, not worst case).
- Analog Devices's AD7546 also uses a segmentation technique, but it requires two external op amps.

Accepting either ac or dc reference voltages over a ±25V range, the HS3160 is TTL and CMOS compatible and includes latchup protection for the digital inputs. It provides an internal current-to-voltage feedback resistor, and its analog output has a 1%-accurate scale factor of 200 μA per reference volt. The output settles a full-scale current excursion in 2 μsec.



Using a segmentation decoding technique, *Model HS3160 16-bit multiplying D/A converter attains 14-bit monotonicity over its specified temperature range. The segmentation also lessens matching and tracking demands on the resistor network.*

Housed in a 22-pin ceramic DIP, the HS3160 comes in four styles: The industrial HS3160C (0 to 70°C); HS3160B (−55 to +125°C; to MIL-STD-883B); HS3160-3 (±0.012% accurate) and HS3160-4 (±0.006% accurate). B and C versions are 14-bit monotonic over −25 to +85°C and 0 to 70°C, respectively. Prices range from $39 to $89 (100).—***Bill Travis***

Hybrid Systems Corp, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 454

Programmable net controller cuts cost of LAN interfacing

By including many system communications functions on chip, the HMOS-III 82586 local-area-network communications controller combines with its manufacturer's 82501 bipolar Ethernet serial interface to replace more than 80 integrated circuits heretofore needed for network interconnection. Conceived primarily to meet Ethernet specifications, the chip set is also programmable to meet the needs of other CSMA/CD (carrier-sense multiple access with collision detection) applications.

The 82586 processes outgoing and incoming packets virtually on its own. After receiving a Go signal from the CPU, it collects messages from shared memory (freeing the CPU for other processing tasks), prepares the packets and controls their transmission without further CPU attention. The device also disassembles incoming packets, checks addresses and errors and stores the messages in memory without CPU intervention.

Tallies errors and diagnoses

In addition to its message-processing functions, the 82586 provides error-status information to memory to be accessed by the CPU at its convenience. If the controller detects an error, it sets the appropriate error-bit flag in memory and can recover the buffer memory without CPU aid. The CPU need only prepare messages for transmission and buffer space for received data—the controller does the rest.

The 82586 also performs systematic diagnostics, allowing you to first check the station's (and chip's) health and then examine conditions from the station to the node. Its built-in time-domain-reflectometer circuit can pinpoint short or open circuits in the network cable.

Program for other LANs

Once initialized, the 82586 automatically assumes the Ethernet parameters: 64-byte minimum frame size, 32-bit CRC (cyclic redundancy check), 6-byte address and 64-bit preamble. You can, however, program the device for other systems. For example, you can call for shorter preambles, smaller minimum packets, shorter slot times and a smaller address space. These changes would suit the chip for less demanding network applications—intelligent subsystem modules interconnected in a serial backplane, for example.

The 82501 Ethernet serial interface replaces eight to 12 components in completing the connection between the host CPU and the network. A combination line driver and receiver, it Manchester-encodes serial data for transmission and filters and decodes received data for the 82586 controller. The interface also contains the system clock oscillator for synchronizing 82501/82586 activity and for supporting the 10M-bps data-transfer rate.

The 82586/82501 combination, coupled with a transceiver, provides the full Ethernet physical and data-link functions. At the transceiver end, the 82501 provides a straightforward interface to an Ethernet transceiver cable. Interfacing with any 8- or 16-bit bidirectional system bus, the chip set requires only two μP connec-

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COMMUNICATIONS DIVISION

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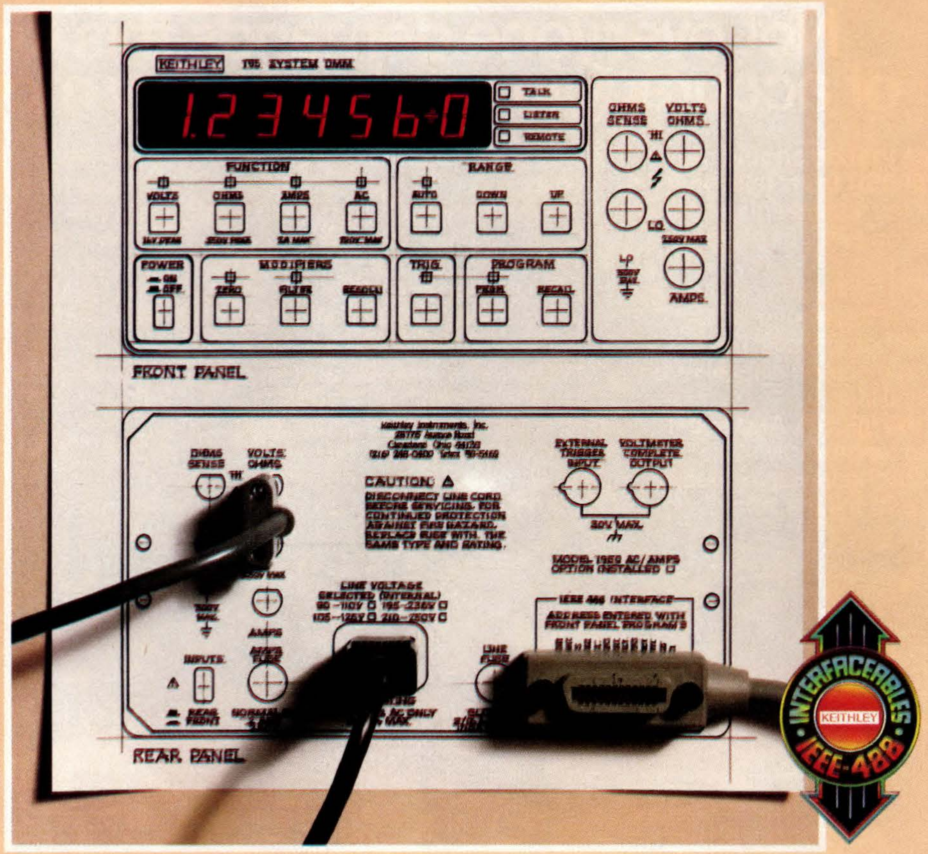
Circle No. 221 for Literature

Circle No. 222 for Sales Contact

A System DMM,



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Your best reason to buy our new System DMM is not the price. Its built-in intelligence provides control—the more you have, the more effective you will be. And the 195 gives you more control than you ever thought possible in an affordable System DMM. The 195 is a full 5-function System DMM with sensitivities of 100nV, 100$\mu\Omega$ and 100pA. Inputs are provided front and back for all functions. Its internal buffer can store up to 100 readings via either the front panel or the IEEE bus. The buffer has 10 selectable rates and can be interrogated for high, low and average readings at any point in time. Digital calibration and a self-diagnostic program minimize down time.

Truly a "set-it-and-forget-it" instrument, the 195 eliminates the need to handle each reading as it is taken. It also eliminates the frustration of doing long, tedious programs for simple, repetitive reading commands. All this control permits you a great deal of freedom in determining various roles for the 195 within your system. In short, our intelligent new 195 offers you more control for improved performance, greater convenience and enhanced cost effectiveness. It is an intelligent device which you won't outgrow as your applications change. Call us for a demonstration of the 195. We'll show you how intelligent it really is — end to end. For only **$995.**

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- Integration period
- ★ Zero
- ★ Filtering
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- Front panel messages
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- ★ Trigger modes
- Service request
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- ★ Digital calibration
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- ★ Talk-only mode
- ★ Resolution
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CIRCLE NO 41

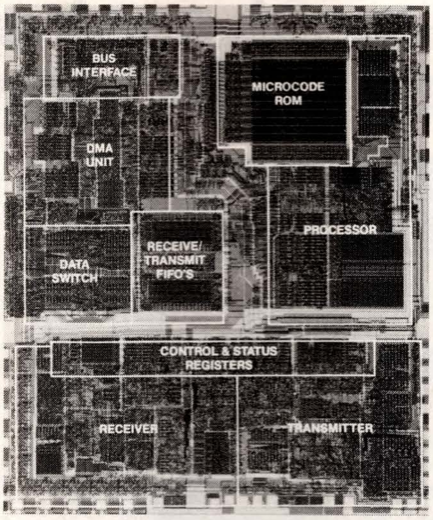
tions: a channel-attention line that lets the CPU wake up the controller and an interrupt line to get the CPU's attention.

Automatic traffic control

When traffic is present on the LAN, the transceiver senses the carrier and signals the 82501 interface unit, which in turn signals the 82586 controller. In the event of a transmission-startup collision, the interface unit alerts the controller, which initiates a jam sequence, turns off the transmitter, performs the backoff-algorithm calculation and attempts retransmission when the backoff waiting time expires.

Seeq's 8001 Ethernet data-link controller (EDN, November 10, pg 82), another entry in the LSI-LAN-controller field, provides functions similar to those of the 82586/82501 set but is dedicated to the Ethernet protocol.

The 82586/82501 LAN-controller set will be available for sampling in 1st qtr 1983; quantity production is slated for the second quarter.



Featuring programmability for non-Ethernet local-area networks *as well as Ethernet compatibility, Model 82586 network controller combines with Model 82501 serial interface to perform all packet-processing functions, freeing the host CPU for more fruitful tasks.*

82586, $65; 82501, $25 (100).

— William Travis

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-7602.

Circle No 455

Modular digital workbench handles analysis, emulation

An uncommitted mainframe that includes three Z80 µPs and an ECL-based bus system combines with plug-in modules to maximize measurement flexibility in the ATLAS (Adaptive Test and Logic Analysis System) integrated digital workbench. Initially available modules handle logic analysis and emulation; future offerings will provide word generation as well as signature, serial-data and waveform analysis.

The $10,000 ATLAS mainframe measures 17.5×27×10 in. and weighs roughly 55 lbs when both module slots are filled. It includes two 150k-byte 5¼-in. double-sided, double-density floppy-disk drives that work in conjunction with one Z80A to support the CP/M operating system.

A second Z80A handles the extensive test and analysis software library available for the manufacturer's stand-alone instruments. The third µC provides multitasking capability, accesses the outside world (to allow the ATLAS to emulate a VT-100 terminal, for example), and also handles RS-232, GPIB and Centronics interfaces.

A 5×9-in. display features split-screen viewing to simultaneously show menus, comments, test results or monitor functions. Seven soft keys to the right of the CRT easily implement special functions that

A modular approach provides maximum measurement flexibility *in ATLAS test systems, which combine plug-in instrument front ends with a CP/M-driven universal computer.*

users write in Pascal and execute on CP/M. Because each module has its own set of functions and commands, the detached ASCII keyboard also contains 18 "flip keys," above which you place a flip card that describes the functions each key initiates for a particular module.

Each front-end subunit contains the hardware *and* software for a specific measurement task; as you insert a plug-in, it downloads its dedicated software into mainframe RAM. Dedicated logic-analyzer modules for the 1802, 6502, 8080, 8085, 6800, 6809 and Z80 µPs will shortly be joined by units for the 68000, 8086, 8088, Z8001 and Z8002.

In addition, you can choose general-purpose logic-analyzer modules that take advantage of the high-speed bus: The series now includes modules with 48 channels at 10 or 20 MHz. (Future introductions will provide 16 channels at 300 MHz and 32 at 200 MHz.) Thus, you can plug in one dedicated unit to track state variables and a high-speed unit for either further state analysis or timing analysis.

Emulation capability is now available for the Z80 and 8085. And because all the necessary hardware resides in the emulator plug-in, the probe itself requires only a small signal buffer. Current plug-ins sell for $2000 to $4000; upcoming high-speed units will cost as much as $10,000.—***Paul G Schreier***

Dolch Logic Instruments Inc, 230 Devcon Dr, San Jose, CA 95112. Phone (408) 998-5730.

Circle No 456

500 Watt Switchers

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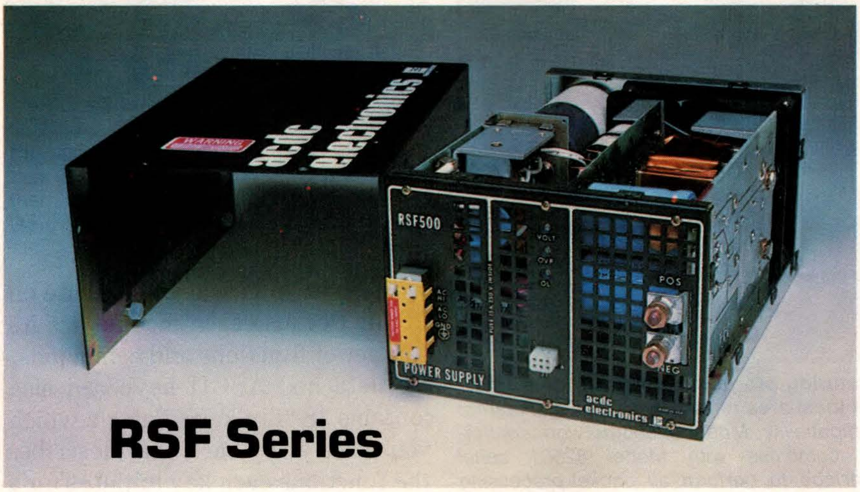

Sub-Modular construction, an ACDC exclusive, assures high MTBF and low MTTR. The latest LSI inverter circuitry, power semiconductors and fault/error detection IC'S reduce parts count for a truly modern, cost effective design. Quality is assured through a 48-hour burn-in and hard copy test data with every unit. RSF units are also available with an optional filter to meet FCC 20780 and VDE 0871 requirements. At about a dollar per watt in OEM quantities, you can't beat it.

Feature	Function	Benefit
Sub-modular construction	Eliminates internal wiring; lowers production cost.	Higher reliability, low MTTR; easy to test and trouble shoot. Lower cost; quick delivery.
Design based on proven product.	The best features of our highly popular "RS" and "EAGLE" series in a new 500W package.	Low risk . . . a new product with proven reliability.
Proportional drive	Switching transistor drive circuit.	Switching Transistor failure does not damage control circuit. Few components, thus higher MTBF and lower cost.
A complete 500W family	Singles, dual, triples and quads.	One supply to replace multiple supplies or upgrade system.
High power dual model	Two 400W channels (500W total max.)	Ideal for CMOS, Micro processors, ECL, or test systems.
External switch for 115/230 VAC	Easy conversion of 115/230 VAC.	Universal usage; no additional cost.

Additional Features and Benefits • Bi-directional forced air • Designed to meet MIL spec shock and vibration in shipping • Inhibit, remote sense, margining, over voltage, over current protection • Extended hold-over • Vacuum impregnated, high frequency shielded magnetics • Low ESR output caps • Inrush protection • Outputs of 2 thru 28 VDC • Options include power fail, crowbar, output out-of-tolerance, VDE0804 hipot, reverse air • 100% screening of primary active devices • Steel chassis and cover provide strength, EMI suppression

RSF 501 SINGLE OUTPUT UNIT	
OUTPUT VOLTAGE	MAX OUTPUT CURRENT IN AMPS
2	100A
5	100A
12	42A
15	35A
24	21A
28	18A
SINGLE OUTPUT $575.00	

RSF 102 HI-POWER DUAL OUTPUT UNIT	
Combine any 2 of the following (500W max.)	
OUTPUT VOLTAGE	MAX OUTPUT CURRENT IN AMPS
2	50A
5	80A
12	33A
15	27A
24	17A
28	15A
HI-POWER DUAL OUTPUT $739.00	

RSF 502 DUAL OUTPUT 500W MAX.		
OUTPUT VOLTAGE	MAX. CURRENT RATINGS IN AMPS	
	OUTPUT 1	OUTPUT 2
2	N/A	16A
5	80A	16A
12	33A	16A
15	27A	14A
24	17A	8A
28	15A	7A
DUAL OUTPUT $650.00		

RSF 503 TRIPLE OUTPUT/RSF 504 QUAD OUTPUT 500W MAX.				
	MAX. CURRENT RATINGS IN AMPS			
OUTPUT VOLTAGE	OUTPUT 1	OUTPUT 2 & 3	OUTPUT 4	SEMI-REG. OUTPUT 4
2	N/A	8A		
5	80A	8A	5A	
12	33A	8A	2A	
15	27A	7A	2A	
24	17A	4A	1A	
28	15A	3.5A	1A	24V @ 4A 6A PEAK
24		*		
TRIPLE OUTPUT $695.00/QUAD OUTPUT $745.00				

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CIRCLE NO 42

High-speed CMOS multipliers suit DSP applications

The introduction of four purely digital ICs from a recognized leader in analog circuitry highlights the increasing use of such devices to perform purely analog functions. In signal-processing applications such as digital filters, Fourier analyzers and image manipulators, you'll find multipliers and multiplier/accumulators (MACs) such as the ADSP 8- and 16-bit CMOS units becoming as important as op amps.

The first CMOS multipliers intended specifically for DSP systems, the ADSP Series devices are pin compatible with TRW TPC and MPY Series bipolar parts. But they typically dissipate 10 to 25 times less power than the TRW devices while operating at approximately the same speed. This performance proves important because multiplication is as fundamental to DSP systems as amplification is to traditional linear circuits: The algorithms that digital filters and matrix processors employ, for instance, rely primarily on accumulated sums of sequential multiplications, so circuit elements capable of adding successive data products constitute a DSP system's core. As a result, multiplier and MAC speed and resolution generally determine signal-processor performance.

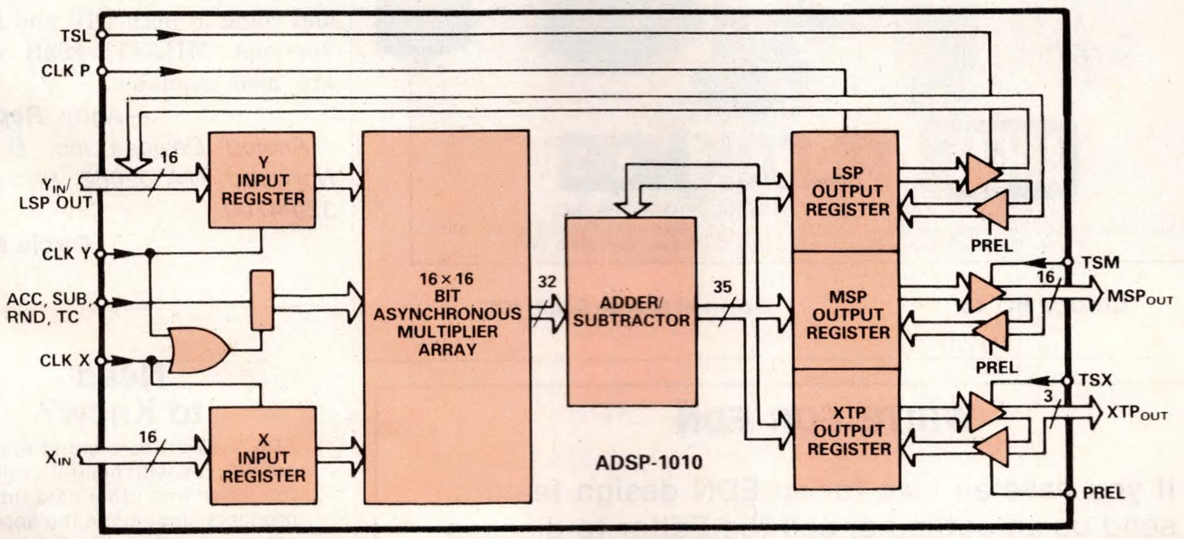
Layout increases speed

According to John Oxaal, marketing specialist at manufacturer Analog Devices, the units' fast operation doesn't derive from exotic fine-line fabrication processes but rather from optimized chip layout. The parts can therefore employ conservative, high-yield 5-μm geometries. They also employ modified Booth algorithms, feedforward carry circuits and conditional final-stage adders to further increase data throughput.

For example, the 16×16-bit ADSP-1016 multiplier executes a clocked-multiply cycle in less than 100 nsec typ and consumes only 150 mW. This $147 (100) device offers the same pinout and functions as TRW's MPY-016HJ, furnishing 32-bit products, compatibility with 16-bit μC buses and optional output rounding to 16 bits. It operates in two's-complement, unsigned-magnitude and mixed modes and includes clocked or transparent output latches.

Providing output accumulation as well as fast multiplication, the ADSP-1010 16×16-bit MAC consumes 175 mW and specs 150-nsec typ cycle time. Compatible with TRW's TDC-1010J, it includes a 35-bit output accumulator divided into two 16-bit product registers and a 3-bit overflow latch.

Each output register includes a preload control that permits you to initialize the accumulator, and the device supports addition or subtraction of current products from preloaded output data. Priced at



For use in signal-processing circuits, *ADSP Series digital multipliers and multiplier/accumulators perform analog functions. This ADSP-1010, for example, couples high-speed operation with low power consumption, providing the core for digital-filter, image-processing and matrix-manipulation systems.*

$198 (100), the part accommodates unsigned-magnitude or two's-complement data formats and features selective 16-bit current-product rounding before accumulation.

8-bit devices

For 8-bit applications, the $45 (100) ADSP-1080 generates 15-bit products from two 8-bit inputs in less than 85 nsec. A low-power second source for TRW's MPY-8HJ, it consumes 55 mW typ and provides 8-bit I/O through two input and two output ports. This device operates on integer or fractional two's-complement data, providing 14 product bits plus a sign code.

The fourth ADSP Series device, the ADSP-1008 8×8-bit MAC functions like the 16-bit ADSP-1010 but provides half that part's resolution. Compatible with 8-bit μPs, it includes two 8-bit input ports and a 19-bit output bus divided into two 8-bit product registers and three overflow lines. This $65 (100) MAC has the same pinout as the TRW TDC-1008J and performs a complete multiplication and accumulation in 95 nsec, dissipating 150 mW.

All four ADSP components provide TTL-compatible inputs and outputs, operate from a 5V supply and come in both DIP and flatpack versions. MIL-STD-883B versions are also available.

—Andy Rappaport

Analog Devices Inc, Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 457

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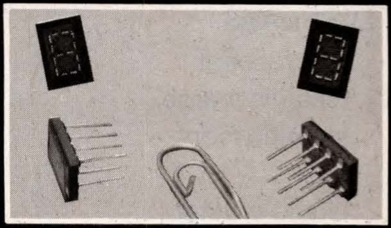

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PLESSEY

CIRCLE NO 44

Leadtime Index

ACTIVE COMPONENTS

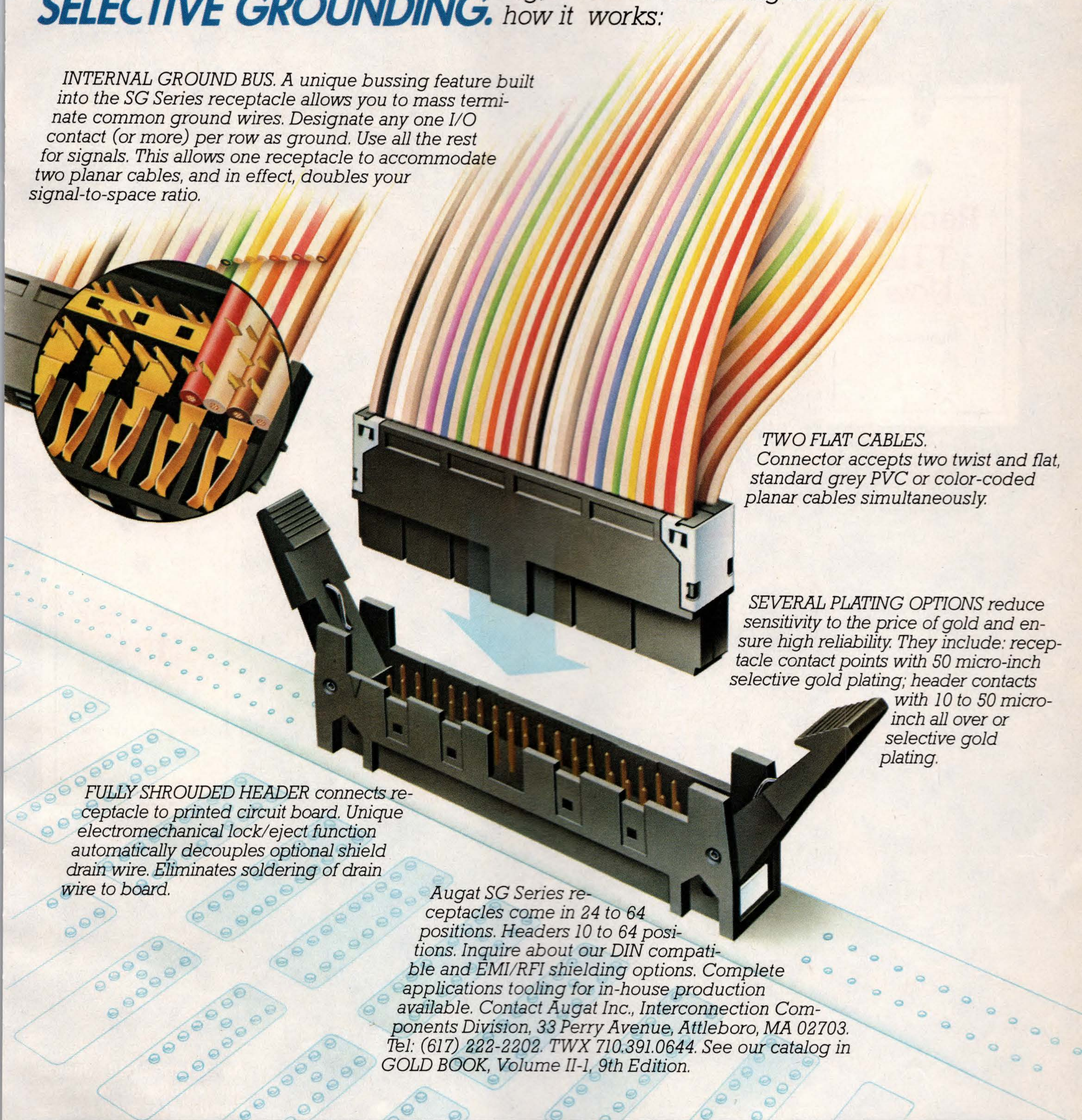
PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
DISCRETE SEMICONDUCTORS			
Diode, switching	2	6	=
Diode, zener	3	4	▼
Rectifier, low-power	2	4	▼
Rectifier, power	4	7	▼
Thyristor, low-power	3	8	▼
Thyristor, power	3	7	▼
Transistor, bipolar power	2	8	=
Transistor, bipolar signal	4	13	=
FET, power	1	6	=
FET, signal	2	6	=
Transistor, RF power	4	10	=
DISPLAYS			
Fluorescent	3	10	=
Gas-discharge	6	9	▼
Incandescent	8	16	=
LED	6	12	=
Liquid crystal	2	10	=
Plasma panel	6	16	=
ELECTRON TUBES			
CRT, black and white TV	7	12	=
CRT, color TV	2	6	=
CRT, industrial	5	18	=
Industrial power	2	10	=
Light and image sensing	2	12	=
Microwave power	6	10	▼
INTEGRATED CIRCUITS, DIGITAL			
CMOS	4	19	△
Diode transistor logic (DTL)	5	12	=
Emitter-coupled logic (ECL)	3	9	=
Low power Schottky TTL	1	7	△
Standard Schottky TTL	1	12	=
Standard TTL	2	6	=
INTEGRATED CIRCUITS, LINEAR			
Communications circuit	2	7	=
Data converter	1	6	=
Interface circuit	4	11	▼
Operational amplifier	4	10	▼
Voltage regulator	5	15	△

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
MEMORY CIRCUITS			
EPROM	2	7	=
PROM, bipolar	5	10	=
RAM, bipolar	3	12	=
RAM, CMOS	2	7	=
RAM, 4k MOS dynamic	2	5	△
RAM, 16k MOS dynamic	4	8	△
RAM, 64k MOS dynamic	5	20	=
RAM, 1k MOS static	2	10	=
RAM, 4k MOS static	4	10	=
ROM, masked MOS	3	12	=
MICROCOMPUTER/MEMORY SYSTEMS			
Core memory board	3	13	=
IC memory board	4	8	▼
Interface board	4	10	▼
Microcomputer board	6	14	=
MICROPROCESSOR IC'S			
CPU, bipolar bit slice	3	6	=
CPU, 4-bit MOS	2	4	=
CPU, 8-bit MOS	4	8	▼
CPU, 16-bit MOS	4	12	▼
Peripheral chip	2	10	=
OPTOELECTRONIC DEVICES			
Coupler and isolator	4	8	=
Discrete light-emitting diode	5	10	=
PACKAGED FUNCTIONS			
Amplifier, instrumentation	5	10	=
Amplifier, operational	6	12	=
Amplifier, sample/hold	4	8	=
Converter, analog/digital	2	8	=
Converter, digital/analog	2	6	=
PANEL METERS			
Analog	4	8	▼
Digital	4	6	△
POWER SUPPLIES			
Custom	15	30	=
Enclosed modular	6	10	=
Open-frame module	10	18	=
Printed circuit	9	16	=

Leadtimes are based on recent figures supplied to *Electronic Business* magazine by a composite group of major manufacturers and OEMs. They represent the typical times necessary to allocate manufacturing capacity to build and ship a medium-sized order for a moderately popular item. Trends represent changes expected for next month.

DOUBLE YOUR SIGNAL-TO-SPACE RATIO WITH AUGAT SELECTIVE GROUNDING.

Now there's an IDC mass termination receptacle and header system that lets you double I/O density on standard-sized printed circuit boards. It's called the Selective Grounding, SG Series from Augat. Here's how it works:



INTERNAL GROUND BUS. A unique bussing feature built into the SG Series receptacle allows you to mass terminate common ground wires. Designate any one I/O contact (or more) per row as ground. Use all the rest for signals. This allows one receptacle to accommodate two planar cables, and in effect, doubles your signal-to-space ratio.

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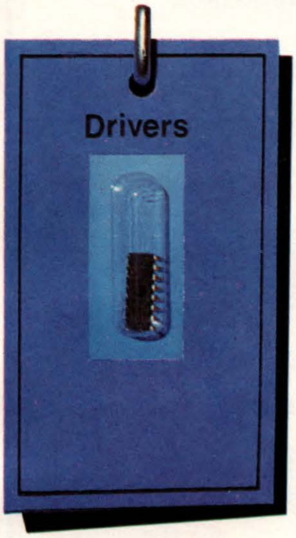
An off-the-shelf design aid remains in wide demand: *TTL is still the prime choice of logic designers who must tie their creations together efficiently and effectively. (Photo courtesy Fairchild Semiconductor Div)*



TTL enhancements and extensions

Classical TTL is far from moribund; it's being extended in a variety of ways. Still, some replacement technologies promise to reduce its appeal in several areas.

Robert H Cushman, Special Features Editor

Transistor-transistor logic (TTL), long prized as a safe and trusted building block for OEM designs, has never been healthier. Although no longer used extensively for total-system design, it remains the primary "glue" that holds digital systems together. Multiple-sourced, readily available TTL devices, described in simple, well-organized catalogs, serve all traditional circuit-design needs. And these SSI and MSI glue-part families are being expanded to meet μP-bus-system needs: The many new octal parts now available exhibit increased speed and decreased power consumption, and they are also less susceptible than conventional parts to damage from such real-world system anomalies as signal overshoot and board removal and replacement with power on.

Furthermore, a whole new world of CMOS "TTL"—high-speed CMOS replacements for low-power Schottky (LS) TTL—is opening up. These devices should prove particularly welcome in all-CMOS systems, and in their TTL-compatible versions, you can use them selectively to reduce system power.

Classical bipolar TTL is supplied by the giants in the semiconductor industry: Texas Instruments, National Semiconductor, Fairchild, Motorola and Signetics, among others **(Table 1).** According to these suppliers, demand is evident for even the older non-Schottky TTL because it has been designed into so many products. In some cases, the devices are used in military programs that have amazing staying power; reorders continue 10 yrs after the initial designs. (Raytheon, for example, still makes the mid-'60s-vintage Sylvania SUHL I and II lines, marketing them as RAY I and II.) In the more recently introduced Schottky TTL, supply has finally caught up with demand. But Fairchild, for one, doesn't see demand for LS TTL used in new designs peaking until 1985.

The end result? Bipolar TTL appears to be the "fabulous invalid" of semiconductors. Everything that was to replace it has only added to its longevity.

For example, the NMOS LSI elements of μP systems were supposed to do away with TTL, but these LSI parts need so much TTL glue that TTL usage has in fact increased with their use. Similarly, the threat to bipolar TTL by the new higher speed CMOS TTL replacements is only making bipolar-TTL suppliers more aggressive in speeding up their processes and circuits to remain ahead of CMOS.

Indeed, bipolar-TTL manufacturers have only just begun to battle the CMOS encroachments. They concede that CMOS's low-power operation might be

TABLE 1—SUPPLIERS OF BIPOLAR TTL

	SUHL ①	74	74LS	FAST	AS	ALS	SPECIAL
TEXAS INSTRUMENTS		•	•		•	•	
NATIONAL SEMICONDUCTOR		•	•		•	•	•
FAIRCHILD		•	•	•			
MOTOROLA		•	•	•	•	•	
SIGNETICS/PHILIPS		•	•	•			
AMD							• ②
RAYTHEON	•						
TELEDYNE							• ③
MMI							• ④

NOTES:
1. HAS NOT BEEN USED IN NEW DESIGNS FOR SOME TIME, BUT INCLUDED TO EMPHASIZE TTL LONGEVITY.
2. MANY HIGH-PERFORMANCE LSI PARTS THAT COULD BE CONSIDERED AS EXTENSIONS OF TTL.
3. HIGH-NOISE-IMMUNITY LOGIC AND POWER-MOSFET DRIVERS.
4. GATE ARRAYS PACKAGED AND NUMBERED AS TTL PORTS.

TTL families expand to accommodate μP-bus uses

unbeatable in applications where most gates switch at 100 kHz or less **(Fig 1),** but that's about all they concede. In fact, some claim that bipolar technology will prove inherently superior for maximum-speed glue parts, delivering more drive per chip area and scaling down more efficiently than does CMOS **(Ref 1).**

The thrust of bipolar-TTL advances varies with the level of integration. At the SSI/MSI level, the emphasis is on improving the basic TTL gate circuit. At the LSI level, the emphasis is on the internal use of other technologies—ECL, STL, I^2L—to obtain very high internal speed at minimum power consumption.

The work at the SSI/MSI level is fairly obvious and easy to understand. The new AS and ALS circuits from Texas Instruments and the new FAST circuits from Fairchild **(Fig 2)** represent attempts to extend Schottky clamping concepts. In these approaches, manufacturers use the increased density allowed by the finer-line processes to add transistors and other circuit features that in turn eliminate some of the shortcomings of conventional TTL. For example, the new circuits can better handle the signal overshoots and undershoots that occur when driving bus lines at high speeds.

Of course, these new refinements increase processing complexity. For example, manufacturers now use more than one type of Schottky metal to obtain different threshold voltages, which in turn allow more precise setting of antisaturation clamping. However, the refinements make the new circuits easier to use at the system level.

Unlike TTL extensions at the SSI/MSI level, though, efforts at the LSI level of integration are more confused. Are they really extensions of the TTL catalog? Or are they rather a totally new development? The answer varies with the supplier (and sometimes with whom you talk to there).

For example, TI and Fairchild say that their LSI parts are a natural extension of the TTL-family concept into the subsystem and system world. Advanced Micro Devices and National, on the other hand, maintain that the TTL concept ceases to have meaning above the MSI level because at that point it's no longer possible to define universal parts of interest to all application areas. These manufacturers say that users should beware of LSI TTL-numbered parts that in fact aren't multisourced—as most users expect TTL devices to be. Indeed, most of the successful bipolar LSI TTL extensions have been marketed separately from the TTL family. For example, the AMD 2900 bit-slice μP and the Signetics 8X300 controller μP weren't presented as extensions of TTL.

The same sort of product-positioning jockeying is now going on in digital-signal-processing (DSP) applica-

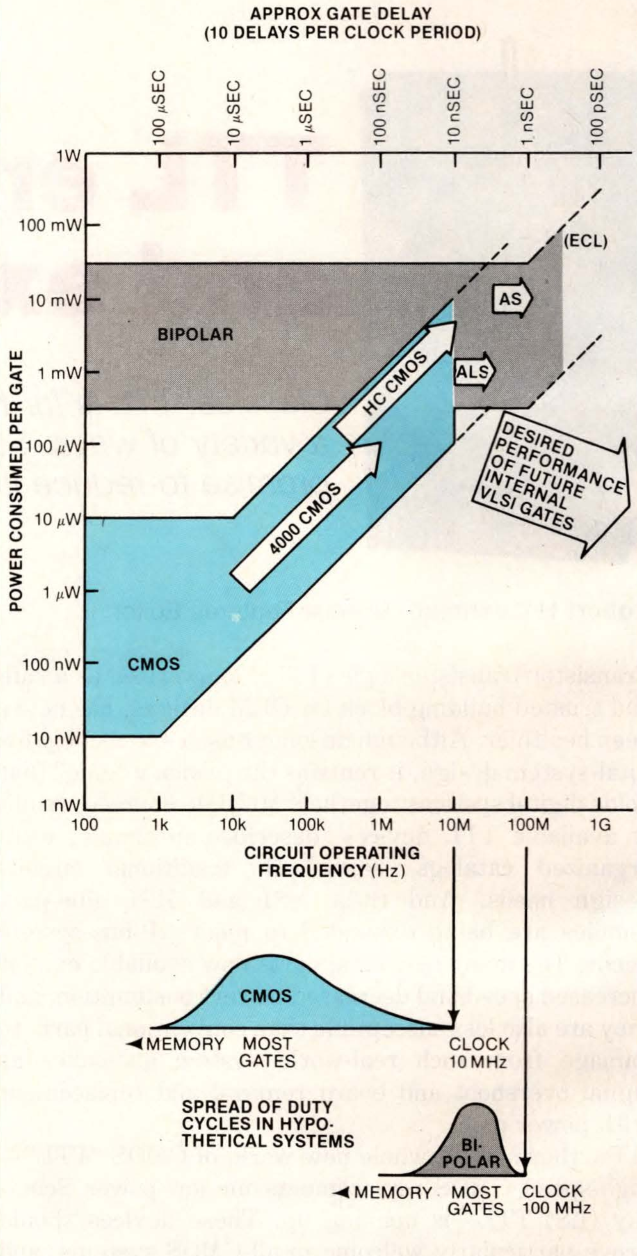


Fig 1—The familiar speed-power curve *provides a good starting point for a quick assessment of the relative strengths and weaknesses of logic-circuit technologies. But although CMOS wins relatively hands down in systems where most of the gates switch at less than 1 MHz and bipolar reigns near 100 MHz, it's not yet clear which technology excels at about 10 MHz. The bell-shaped curves portray the scatter of gate speeds in two possible applications, one suited to CMOS and one to bipolar. They emphasize that most of the gates in an application switch at a fraction of the clock rate. Note, however, that the scatter of gate speeds is purposely shown different in each case: For the CMOS case, the diagram assumes that most gates switch much more slowly than the clock; for bipolar, most switch at rates closer to the clock speed. The different speed-power characteristics of the two technologies make these the optimum approaches.*

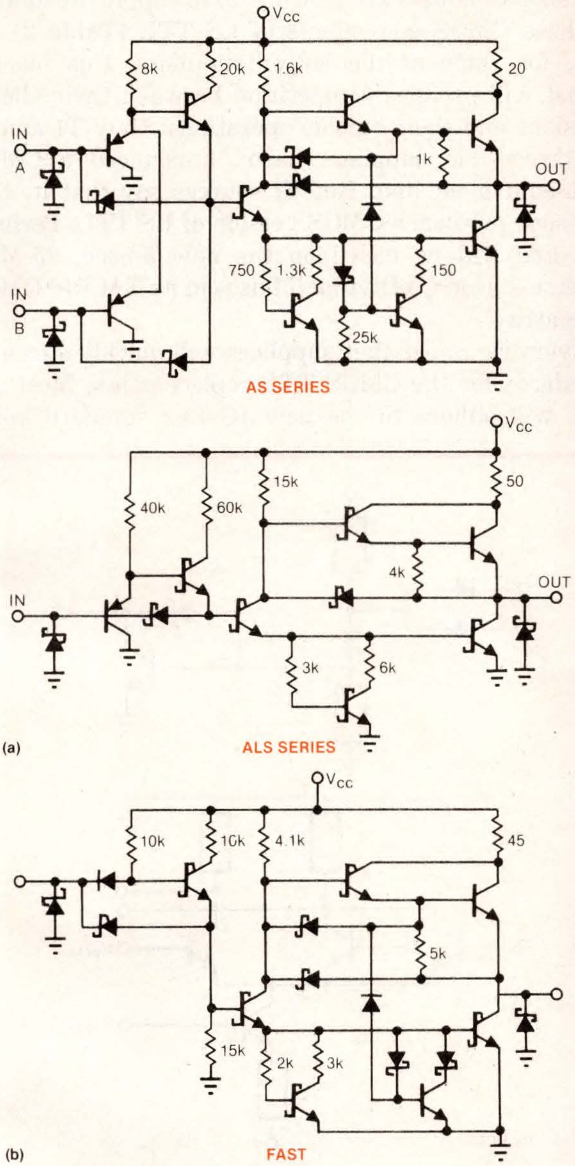


Fig 2—Improved bipolar TTL gates *from Texas Instruments* ***(a)*** *and Fairchild* ***(b)*** *use new processing techniques such as oxide isolation (to reduce capacitance) and smaller geometry (to increase transistor performance and packing density). These newer forms of TTL provide improved speed-power products and improved tolerance to noise and supply-voltage overshoots and undershoots. And because the devices need less input current, fanout is also improved. The TI AS Series aims at all-out speed (2-nsec delay) and is therefore somewhat power hungry (10 to 20 mW). The ALS Series endeavors to better the widely used LS TTL in terms of both speed and power. And FAST (Fairchild Advanced Schottky TTL) is similar in intent to TI's ALS; it uses 2-μm geometry and oxide isolation to increase LS speed fourfold while only doubling LS power consumption. All of these circuits are more complex than the original TTL, but their manufacturers say that modern finer-line processing allows them to occupy about the same die area. At any rate, the price of TTL has dropped so low that the silicon cost is overshadowed by the packaging cost.*

tions. Here, TRW and AMD have taken a lead in very fast MSI/LSI-level building blocks such as TRW's multipliers and AMD's 29500 family—neither of which is termed a TTL extension. TI and Fairchild, on the other hand, say they are targeting the DSP area as one in which they can extend their TTL dominance. In some instances they might duplicate functions originated by AMD and TRW—and renumber those functions into their own TTL nomenclature.

Is TTL needed at the LSI level?

Regardless of which family the makers of these bipolar LSI parts say the devices belong to, the devices appear to have two characteristics:

- They retain bipolar-TTL I/O compatibility.
- They use circuitry other than TTL internally.

The contradiction between these two characteristics could eventually produce discord that in turn will lead to the end of the TTL era. The reason? Although the first characteristic, the retention of TTL I/O compatibility, is rapidly becoming LSI devices' only link with TTL, the second characteristic is separating the new devices from conventional TTL.

For example, many of the new parts' internal circuits use supply voltages lower than the TTL 5V standard to provide lower power dissipation. And the circuits' internal signals don't exhibit TTL's peculiar lopsided swings, either; ECL circuits, for instance, show relatively lower amplitude and symmetrical swings.

The various suppliers also favor different internal circuits (**Fig 3**), further blurring the link with conventional TTL. National and AMD, for example, use ECL for their 2900 bit-slice-μP families. TI, on the other hand, uses STL, an improvement on I^2L, in its advanced AS800 and ALS800 Series LSI parts (which include the 888 8-bit-slice ALU). And Fairchild's R&D Center (Palo Alto, CA) has been using its proprietary I^3L for the 9445 μP and Fairchild's new family of DSP circuits, which could lead to I^3L's use in future FAST LSI circuits as well. In many cases, these are the same internal circuits used in the supplier's gate arrays.

CMOS TTL extends bipolar's life

Will users view these new LSI bipolar parts as TTL extensions? Will they care how the parts are characterized? Time will tell. Meanwhile, the new CMOS equivalents of LS TTL could give the low-level SSI/MSI TTL glue parts an extended life, even though they use different internal circuits, have different signal swings and support lower supply voltages.

Manufacturers of these CMOS TTL replacements appear confident that the CMOS parts will replace LS TTL in the large, established SSI/MSI glue-part market. Most of the major semiconductor houses and a

CMOS substitutes spur TTL makers to extend their lines

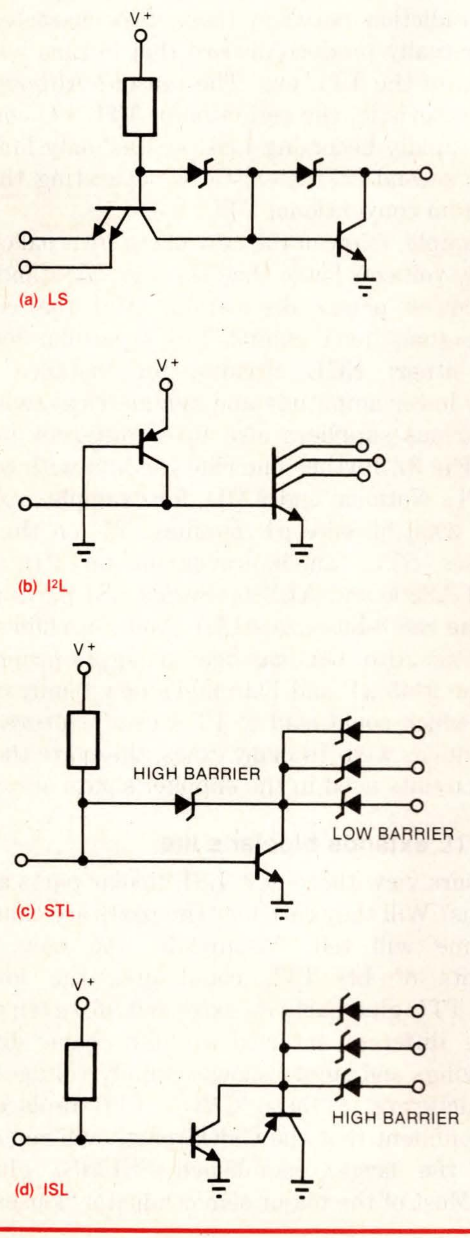
TABLE 2—SUPPLIERS OF CMOS LOGIC

	SC ②	74HCT ③	74HC ④
RCA		●	●
MOTOROLA		●	●
NATIONAL SEMICONDUCTOR		●	●
MITEL	●	●	
SIGNETICS/PHILIPS		●	●
FAIRCHILD			●
SEMI PROCESSES	●		●
GTE	●		
SUPERTEX	●	●	
SOLID STATE SCIENTIFIC		●	

NOTES:
1. OLDER 4000 AND 74C SERIES NOT INCLUDED.
2. SC WAS ORIGINAL MITEL DESIGNATION. IT HAS TTL INPUT LEVELS.
3. HCT IS SIMILAR TO SC BUT ADHERES TO PROPOSED JEDEC STANDARD.
4. HC IS PROPOSED JEDEC STANDARD FOR CMOS INPUT LEVELS.

few smaller houses are gearing up to supply broad lines of these CMOS equivalents of LS TTL **(Table 2)**. In fact, for some of the larger suppliers, this market thrust will produce competition between their CMOS divisions and their bipolar operations. Only TI among the broad-line suppliers hasn't announced a CMOS TTL-equivalent line. But TI sources say that it, too, will soon produce a CMOS version of LS TTL. Perhaps this line will be based on the new 5-nsec, 25-MHz reverse-silicon CMOS that TI uses in its TAC010 CMOS gate array.

Everyone hopes that suppliers will quickly agree on standards for the CMOS TTL replacements. Most say they will adhere to the new JC-40.2 standard being



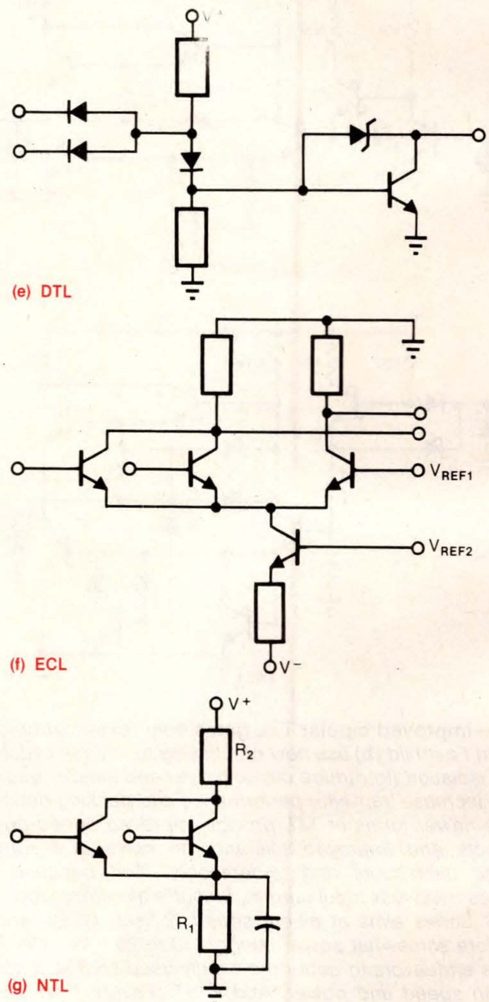


Fig 3—Different types of bipolar gates *are being considered for use in LSI and VLSI circuits. The objective is to gain or maintain nanosecond speed but at greatly reduced power. Various marriages between circuit types and processing technologies include LS* ***(a)****, I²L* ***(b)****, STL* ***(c)****, ISL* ***(d)****, DTL* ***(e)****, ECL* ***(f)*** *and NTL* ***(g)****. These diagrams come from* ***Ref 1****, which is recommended as an excellent overview.*

developed through JEDEC. Standards or no, however, the new high-speed CMOS won't replace LS TTL overnight; several years will pass before all of the hundreds of SSI and MSI parts needed to replace LS TTL are fully prime and second sourced. And it will be several more years before system designers overcome their inertia. Thus, CMOS shouldn't replace LS TTL in a large way until about 1990.

The replacement process won't be without its problems, either—especially in bused systems. For example, how can line terminations be added without increasing CMOS's power consumption and reducing its fanout? And how are CMOS inputs to be kept from drifting when the bus is floating? Considering the latter question proves important if you want to maintain CMOS's low quiescent power and keep the logical states of a system at their proper, known values.

An excellent summary of the design considerations arising when you use CMOS in bused systems appears in **Ref 2.** With regard to terminations, this work suggests using 1- to 100-kΩ resistors, to which you add capacitor networks in certain cases. A better approach, however, might be to use active terminators, such as the 40117B that RCA offers for its older 4000 CMOS logic family, and to make the input gates of CMOS devices controllable, so the devices remain in a known state—as Harris has done on the 82C82, its CMOS version of the Intel 8282 octal latch. (In the 82C82, one

Where is TTL glue used?

TTL glue parts find a variety of uses in system designs. A few of the key ones:

- **Clock oscillators.** A design must often have a separate clock oscillator, even when the μP has its own on-chip oscillator. Typically, a pair of TTL inverter gates serves this need, with the spare gates in the package functioning as output buffers. Sometimes, some divide-by-2 flip flops lower the frequency for various portions of the system.
- **Buffers, bus drivers and address decoders.** Bipolar TTL has long been favored in NMOS systems for adding drive capability to bus lines, particularly when large backplanes must be driven. Octal drivers and transceivers are widely used for this purpose. And the new 16-bit μC systems, because they must be fast and often have backplanes into which a varying number of add-on boards can plug, are demanding bipolar drives—a function that the new AS and ALS TTL drivers provide.
- **Architectural transformers.** You might require logic to modify a μP's bus structure so it can drive memories and peripherals intended for a different bus. Bipolar and CMOS might both serve this purpose, depending on system speed.
- **Start/stop controls.** External circuits used to control the startup and shutdown of μCs and other LSI-level systems can require the use of SSI parts. And CMOS-system hibernation might call for external control via CMOS SSI devices.
- **I/O interfaces to the real world.** An example of this function is the use of 7-segment display drivers.

LSI/VLSI-chip designers are constantly trying to eliminate all these uses of TTL; in each use category, you can find cases where the function has been put on an LSI or VLSI chip. For example, some on-chip clock oscillators permit use of a variety of frequency-control methods, ranging from crystals to resonators to RC networks or even to simple resistors. And bus drivers have been eliminated by consolidating more of the system onto single chips. Single-chip μCs don't need off-chip data-, control- and address-bus drivers, for example, because they have their memory on chip.

In addition, the problem of matching bus architectures is being solved by built-in multimode logic. With this provision, the control-bus signals can be altered by either masking or pin commands. Startup and shutdown controls, meanwhile, are also being built into some of the new μP chips: The Motorola 146805, for instance, has the ability to stop and restart itself. Finally, quite a few 1-chip μCs now have built-in UARTs for serial ports, others incorporate A/D converters, and still others have sophisticated LCD drivers.

Impressive as these on-chip attempts to eliminate TTL glue are, however, they never do in fact eliminate the need for TTL glue in all designs. OEM system designers always seem to want some additional functions, some extra flexibility, that the on-chip solutions don't offer. Thus, experts agree that the total replacement of TTL glue parts is definitely not in sight.

TTL's future at the LSI level remains uncertain

of the p transistors in the CMOS input NOR gate is disabled when the strobe goes HIGH.)

Ref 2 also points out that users who buy at the board level will be facing a confusing situation with regard to CMOS TTL replacements: Some boards will employ 74HCXX glue parts, some will have 74HCTXX glue, and some will use LS TTL glue (see **box,** "What input level for CMOS?"). Each type might have different logic swings, terminations and antifloat provisions. And each might require unique terminations when plugged into a backplane. Imagine how this confusion will grow as the boards are maintained in the field and repair technicians inadvertently plug in boards of the wrong type and replace glue parts of one type with those of another.

TTL versus gate arrays

CMOS devices might eventually replace LS TTL at the SSI and MSI levels. But as noted, the situation at the LSI level is considerably more uncertain. And here, most experts believe that gate arrays will provide the means whereby TTL glue parts will merge into LSI. They feel that NMOS LSI/VLSI technology is causing designers to use TTL glue parts in such a scattered and random manner that it will prove impossible for TTL suppliers to define standard LSI-level TTL parts; TTL in effect is stymied at the MSI level. Gate arrays, however, will allow designers to gather up all their TTL SSI/MSI functions into a single LSI package. For examples of gate-array suppliers using both bipolar and CMOS technologies, see **Table 3** and **Ref 3.** And for an example of how a bipolar gate array replaced 20 TTL packages in a very-high-volume consumer product, see **box,** "Gate arrays eliminate TTL glue in a high-volume product."

Any designer who expects annual production volume greater than 1000 units should consider converting a design to gate arrays. The process involves an up-front cost of about $50,000 and a turnaround time of 6 to 8 wks. Per-part cost for the gate array ranges from $5 to $20, depending on volume.

Note, however, that there seem to be two opinions on how to actually design gate arrays. Advocates of a practical approach say a gate array should represent a collection of uncommitted TTL-like gates on one chip that a designer can use to literally duplicate an existing TTL design. These experts say designers should do their initial design and breadboarding with TTL parts, as before, and then use an array containing the equivalents of these parts (or at least a CAD system that would operate in the TTL-part language).

Advocates of a "purer" approach, on the other hand, say that progressive designers should no longer bother with the TTL prototyping stage at all: They should go directly to their CAD systems to produce gate-array designs. This approach starts with high-level definitions of design objectives. Breadboarding occurs via computer simulation, and prototyping is done on first samples from the array vendor.

In this purist point of view, designing by picking parts from a TTL catalog is woefully crude and archaic.

TABLE 3—REPRESENTATIVE GATE-ARRAY SUPPLIERS

	BIPOLAR	CMOS
TEXAS INSTRUMENTS	•	•
RCA		•
MOTOROLA	•	•
NATIONAL SEMICONDUCTOR	•	•
MITEL		•
SIGNETICS/PHILIPS	•	
FAIRCHILD	•	•
SEMI PROCESSES		•
MONOLITHIC MEMORIES	•	
RAYTHEON	•	
FERRANTI	•	
APPLIED MICROCIRCUITS	•	
INTERNATIONAL MICROCIRCUITS		•
CALIFORNIA DEVICES		•
HARRIS SEMICONDUCTOR	•	

What input level for CMOS?

The use of CMOS equivalents for bipolar TTL functions promises to introduce a few complications into an already somewhat muddled picture. For example, HCT Series CMOS devices (74HCTXX) have their inputs skewed to make them compatible with TTL voltage swings. HC Series devices (74HCXX), however, have their inputs centered for use in all-CMOS systems. (The HCT skewing results from unbalancing the CMOS circuitry's pn input pair or from forming a Schmitt trigger at the input.) Meanwhile, the original high-drive, high-speed CMOS glue parts from Mitel—the 74SCXXX Series—also have skewed inputs that allow them to switch near the 1.4V off-center point of TTL rather than the 2.5V mid-center point of CMOS.

RCA says it originally intended only to produce the HC Series (as Motorola and National do). But feedback from customers convinced it of the need for TTL-compatible CMOS as designers switch from bipolar TTL to CMOS TTL equivalents. Motorola and National now say that they will also produce at least some HCT parts. And Mitel and its second sources report that they'll produce versions of their original SC parts that agree with the HCT standard. Moral? When substituting CMOS for classical bipolar TTL, you should be able to get precisely what you need. But be sure you know what you need.

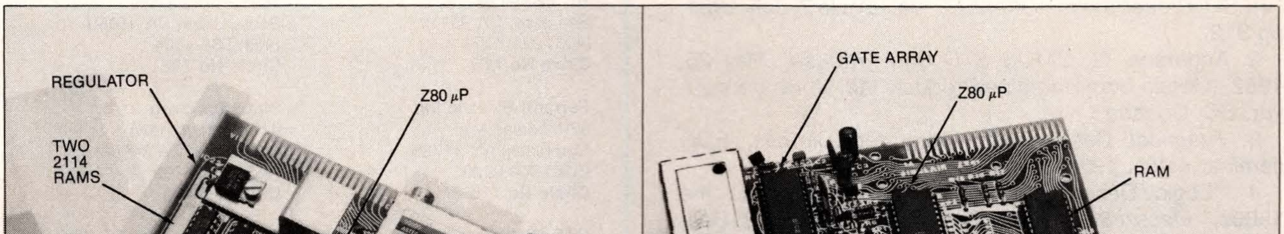
Gate arrays eliminate TTL glue in a high-volume product

In some designs, a gate array can efficiently and economically replace assorted SSI and MSI TTL. In the Sinclair personal computer, for example, designers had to combine 17 TTL parts in one package to achieve a retail price of less than $100. Use of a gate array solved the problem.

The functions to be integrated were unusually diverse, including an oscillator for the computer's Z80 μP, a video interface (US and European TV standards), two cassette interfaces and memory-control circuitry. The designers used a Ferranti bipolar gate array, partially because the Ferranti process accommodates some linear circuits and partially because it's sufficiently simple to reliably turn out millions of units per year (it requires only six steps).

According to Ferranti, this application represents a design situation where a gate array is as economical as a full-custom solution, even if volume rises into the tens of millions of units. The reason? A large number of functions are being integrated, and each requires its own I/O. The final chip size (130 mils square) was determined by the number of required pads, and even though using a fully custom design would have produced a 30 to 40% smaller active area than that of the gate array, the chip size would have remained the same.

Although Sinclair won't release actual cost figures, EDN speculates that the gate array costs $0.01 per gate. For 500 gates, this comes to $5. At the millions-of-units-per-year sales level, this price should drop below $5.



Seventeen LS TTL glue parts *(gates, latches, drivers, etc) combine with a Z80 μP, a 24-pin ROM and two 2114 RAMs in Sinclair's original design for its ZX80 personal computer* ***(a).*** *The redesigned unit* ***(b)*** *uses only four ICs: the Z80, the 24-pin ROM (in a byte-wide 28-pin socket for future expansion), a 4118 byte-wide RAM and a Ferranti ULA 810 2 gate-array IC.*

CMOS parts could eventually replace SSI/MSI TTL

Note, though, that full-custom vendors (such as VLSI Technology) go the array vendors one better: They argue for replacement not only of SSI/MSI TTL, but also of LSI/VLSI NMOS chips. They say that an entire design should be produced from scratch at a CAD terminal and sent off to a silicon foundry, which would then return the result as a single chip.

One scenario that could arise from these considerations has designers start by creating arrays as TTL replacements and then, as the CAD tools for arrays and custom logic are further developed, switch gradually to the higher level approaches that bypass traditional TTL design. But regardless of how quickly and completely design methodology migrates to higher levels of CAD, the jellybean TTL glue parts will in some way persist in most designs—especially those with annual production volumes less than 10,000 units. **EDN**

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Article Interest Quotient (Circle One)
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For more information...

Fast-changing technology, especially in gate arrays, precludes an all-inclusive listing of manufacturers. For more information on the bipolar and CMOS TTL derivatives mentioned in this article and on gate arrays that are extensions of TTL, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. You can also refer to **Tables 1, 2** and **3** for guidance on each firm's product offerings.

Advanced Micro Devices
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Fairchild Semiconductor
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Circle No 714

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Commack, NY 11725
(516) 543-0200
Circle No 716

GTE Microcircuits Div
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
Circle No 717

Harris Semiconductor
Box 883
Melbourne, FL 32901
(305) 724-7000
Circle No 718

International Microcircuits Inc
3350 Scott Blvd
Santa Clara, CA 95051
(408) 727-2280
Circle No 719

Mitel Corp
Box 13089
Kanata, Ontario,
Canada K2K 1X3
(613) 592-5280
Circle No 720

Monolithic Memories Inc
1165 E Arques Ave
Sunnyvale, CA 94086
(408) 739-3535
Circle No 721

Motorola Semiconductor
5005 E McDowell Rd
Phoenix, AZ 85008
(602) 244-6900
Circle No 722

Motorola Semiconductor
3501 Ed Bluestein Blvd
Austin, TX 78721
(512) 928-6800
Circle No 723

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 721-5000
Circle No 724

Raytheon Semiconductor Div
350 Ellis St
Mt View, CA 94042
(415) 968-9211
Circle No 725

RCA Solid State Div
Rte 202
Somerville, NJ 08876
(201) 685-6000
Circle No 726

Semi Processes Inc
1885 Norman Ave
Santa Clara, CA 95050
(408) 988-4004
Circle No 727

Signetics Corp
811 E Arques Ave
Sunnyvale, CA 94086
(408) 739-7700
Circle No 728

Solid State Scientific Inc
Commerce Dr
Montgomeryville, PA 18936
(215) 855-8400
Circle No 729

Supertex Inc
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Teledyne Semiconductor
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Mt View, CA 94043
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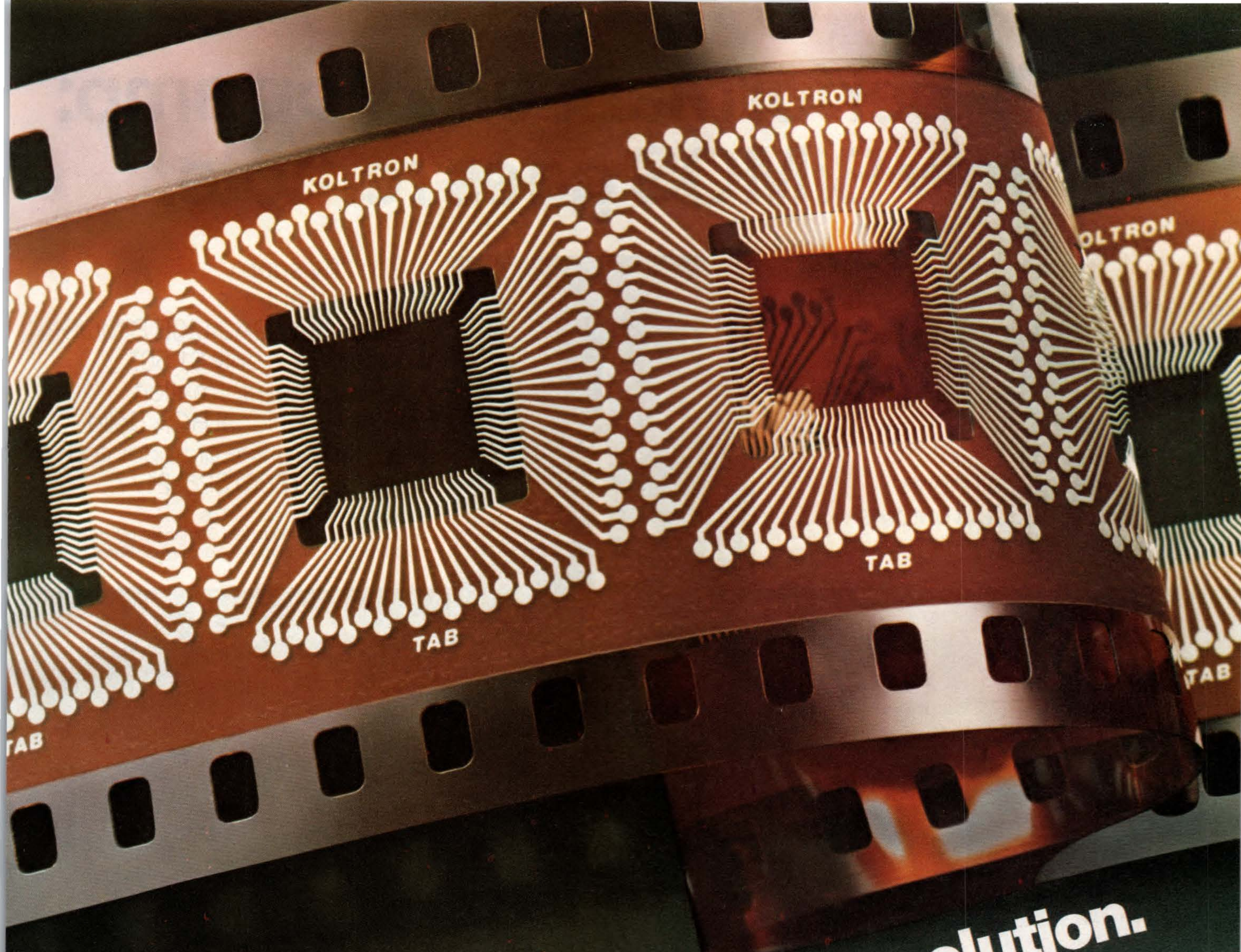

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Logic-compatible MOSFETs simplify high-power interfacing

Combining power MOSFETs with logic-level devices allows you to meet requirements for high-power, high-speed switching while minimizing cost and circuit complexity.

Ed Oxner and **Richard Blanchard,** Siliconix Inc

Able to provide a direct interface between logic-level circuits and high-power loads, power MOSFETs handle high voltage and current while achieving fast switching speeds. But why bother with MOSFETs when so many TTL and CMOS interface circuits are available? The answer is quite simple—TTL and CMOS alone can't do the job.

Consider, for example, that although many TTL peripheral circuits are excellent high-speed, high-current drivers, load-voltage levels above 4.5V rule out their use. CMOS interface circuits can operate at voltage levels to 15V or more, but they in turn have serious current limitations. Thus, you can only use TTL or CMOS to satisfy high-voltage/high-current load requirements by adding complex circuitry that increases cost while decreasing reliability.

MOSFETs circumvent these problems: In addition to having desirable power, speed and interface capabilities, these multisourced devices exhibit rugged thermal characteristics and are immune to hot spotting, secondary breakdown and thermal runaway.

A look inside the package

MOSpower is the generic name for a large family of MOSFETs that includes devices capable of handling power levels from milliwatts to kilowatts. Regardless of power capability or vendor, all devices perform similarly and have an identical cross-sectional structure (**Fig 1**)—a DMOS (double-diffused MOS) configuration with both n and p diffusions in an n-doped substrate. Although it resembles a bipolar structure, subtle processing techniques help it develop operating characteristics quite unlike those of classical bipolar transistors. The differences involve the oxide-insulated gate—usually a polysilicon gate—and a bridge connecting the source to the body. This bridge effectively mutes any parasitic bipolar action that would otherwise result from the npn diffusion profile.

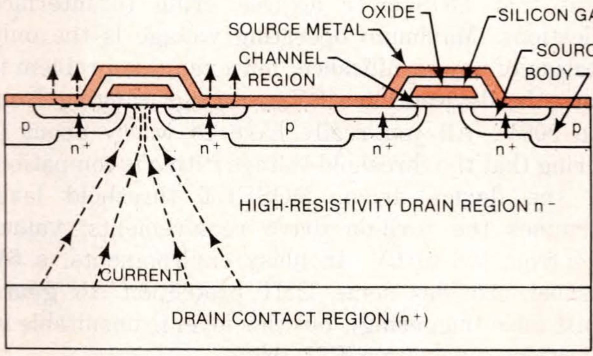


Fig 1—With drain-to-source current uninterrupted by pn barriers, *a power MOSFET exhibits a positive temperature coefficient. Because this characteristic limits current with increasing temperature, a MOSFET has no thermal runaway.*

With a positive bias potential applied to the gate of the **Fig 1** n-channel MOSFET, the p well immediately beneath the gate inverts. That is, the positive gate potential attracts and accumulates a heavy concentration of negative charges under the oxide, converting the p region into an n region and generating a drain-to-source current flow. The pn diode between the body and drain represents the only parasitic element in this DMOS structure. And reverse bias often makes this parasitic element more beneficial than detrimental.

Because gate potential rather than base injection (as in a bipolar transistor) controls conduction, a MOSFET has no minority carriers and hence no minority storage time. Therefore, unlike a bipolar transistor, a MOSpower FET has very-high-speed switching capability

MOSFETs' positive TCs prevent thermal runaway

regardless of its current or voltage ratings. And because it's a majority-carrier device (drain-to-source current flow), a power MOSFET also has a much larger safe operating area. As a result, it can simultaneously switch high voltages and currents with less chance of failure than can a bipolar transistor with an equivalent power rating.

Given its structure, a MOSpower FET can be considered a bulk semiconductor device; that is, with its drain-to-source current uninterrupted by pn barriers, the device has a positive temperature coefficient, and as temperature increases, bulk resistance also increases, creating a form of self protection. Unlike a bipolar power transistor, a MOSFET tends to limit current with increasing temperature, so it experiences no thermal runaway or latching problems.

Taking the work out of interface designs

The presence of few operating restrictions is a prime benefit that MOSpower devices bring to interface applications. Maximum operating voltage is the only limitation of any significance, but even this problem is minor—the devices have BV_{DSS} ratings ranging from 30 to 500V. All you really have to worry about is ensuring that the threshold-voltage rating is compatible with the device drive. MOSFET threshold level determines the turn-on drive requirements; values range from 0.8 to 6V. In noisy environments, a 6V threshold provides some EMI protection (to guard against false triggering), but this level is unsuitable in applications involving a TTL drive.

Like bipolar power transistors, MOSpower FETs are charge-transfer components, so you have to inject or withdraw a finite amount of energy to operate them. However, although you must maintain a steady charge to keep a bipolar unit active, a MOSpower device only requires a charge injection at turn-on. This phenomenon is the key to the MOSpower device's ultra-high-speed switching capability. With no minority-carrier storage time, switching time depends entirely on how rapidly you can transfer a charge in and out.

Because a MOSFET's control gate is insulated from the body, the value of input capacitance (comprising gate-to-source plus Miller-effect capacitance) sets the turn-on charge requirements. Therefore, switching time is a function of charge transfer, effective gate resistance and the input time constant determined by generator impedance and input capacitance.

By fully satisfying drive requirements, you can readily realize low-nanosecond switching speeds using MOSpower FETs. Gate resistance partially limits maximum speed, and the lead inductance of typical packages becomes a limiting factor in the low-nanosecond range. To avoid such limitations, be sure you

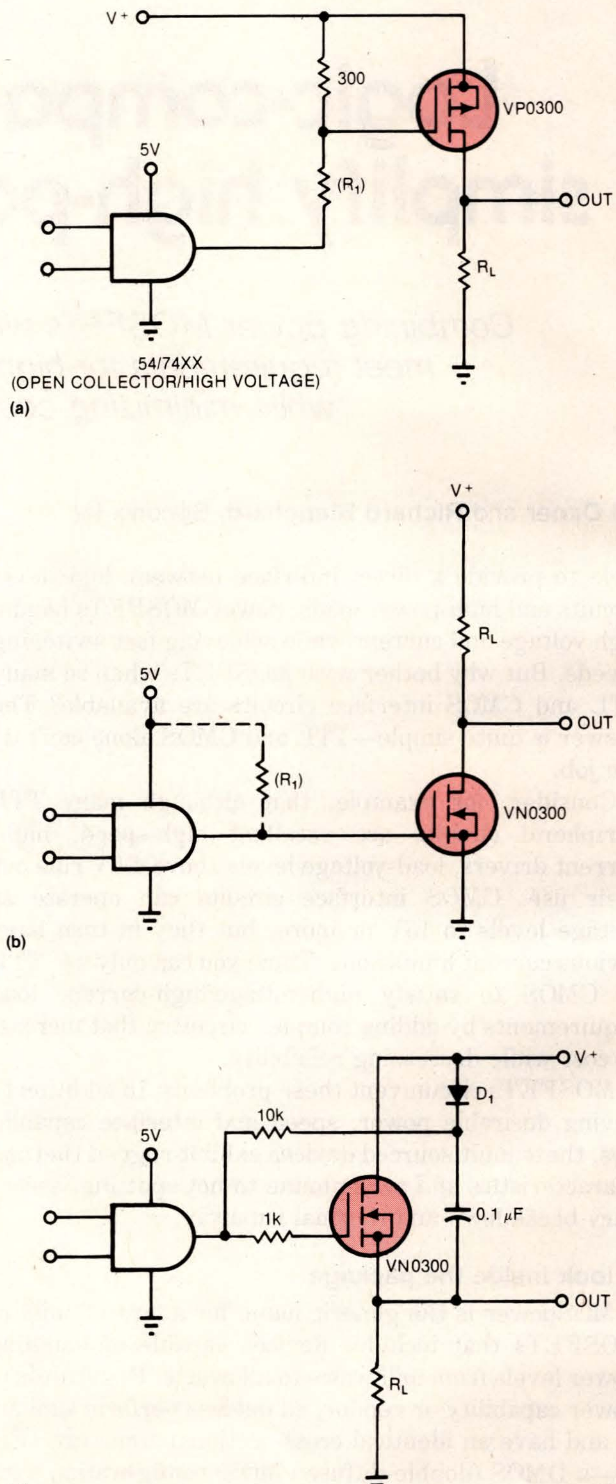


Fig 2—In simple MOSFET interface circuits, *you can turn the device ON with either LOW* ***(a)*** *or HIGH* ***(b)*** *gate signals. The bootstrap circuit* ***(c)*** *suits applications requiring momentary activations.*

specify high-frequency power packages, which solve lead-inductance problems—metal-gate, high-frequency MOSpower FETs are one such choice for applications involving high-speed switching.

Some MOSFET application tips

MOSpower FETs are enhancement-mode devices, so you must bias the gate beyond the source potential for turn-on—more positive for n-channel units and more negative for p-channel devices. Because they are available in both n- and p-channel configurations, you can solve many interface problems using only one device (**Fig 2**).

For example, you can employ straightforward gate-to-FET connections to effect FET turn-on with either LOW or HIGH gate input signals. In the circuit for the p-channel device (**Fig 2a**), R_1 limits load current and equals 600Ω for a 15V FET supply voltage. Although R_1 is not needed in the n-channel circuit (**Fig 2b**), you can use it to balance turn-on and turn-off times.

For applications requiring momentary activation, you can employ a bootstrap circuit (**Fig 2c**) to provide the necessary positive gate bias during turn-on. Here the MOSFET is OFF when the gate is LOW, and the capacitor charges to the rail potential through the diode and load resistance. When the gate input goes HIGH, the FET conducts and raises the source potential. Capacitor charge increases to the source potential back-biasing the diode and applies a positive potential to the gate to ensure full turn-on.

In all cases, consider maximum operating voltage and current limitations as well as switching times. If the application involves ultra-high-speed switching, you need a driver that can rapidly transfer large amounts of current to and from the FET's gate.

Satisfying multiple-device applications

You can stack MOSpower devices in totem-pole, H-bridge or complementary driver circuits. There are at least three circuit variations for a totem-pole driver (**Fig 3**). In each case, the uppermost device drives the lower device, which serves as the load. As a result, you must bias the upper device at a potential higher than the rail to realize full turn-on. This action requires either two supply rails (**Fig 3a**) or use of a bootstrap connection (**Fig 3b**). In the latter case, a HIGH input turns Q_1 and Q_2 ON, and the capacitor charges through the diode and load. When the input goes LOW, Q_1 and Q_2 shut down, and Q_3's gate voltage immediately begins to rise, increasing conduction through Q_3 and raising the potential across the load and Q_2. At this point, the bootstrap begins to operate as in **Fig 2**.

You can increase the bootstrap totem pole's speed by adding Q_4 and D_2 (**Fig 3c**). Q_4 increases the gate

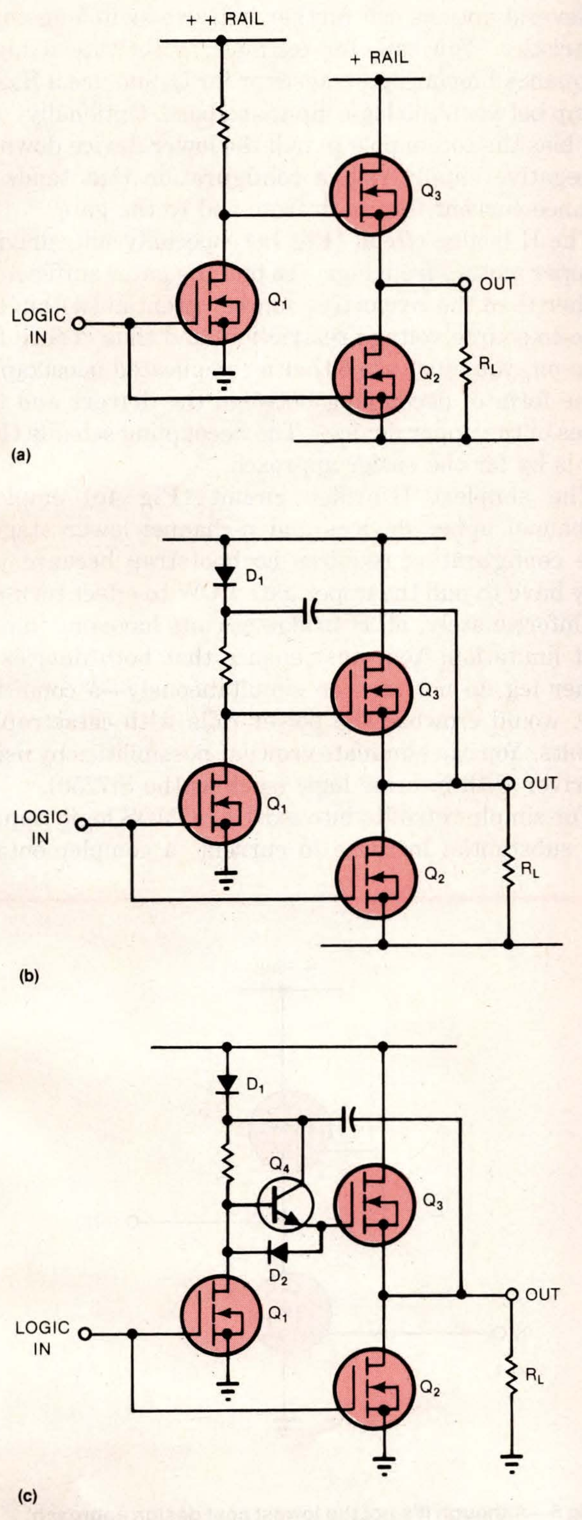


Fig 3—To completely turn the upper devices ON *in totem-pole circuits, use two supply rails* **(a)** *or a bootstrap technique* **(b)**. *Adding Q_4 and D_2* **(c)** *speeds the bootstrap totem-pole response.*

H-bridge configuration suits stepper-motor drive

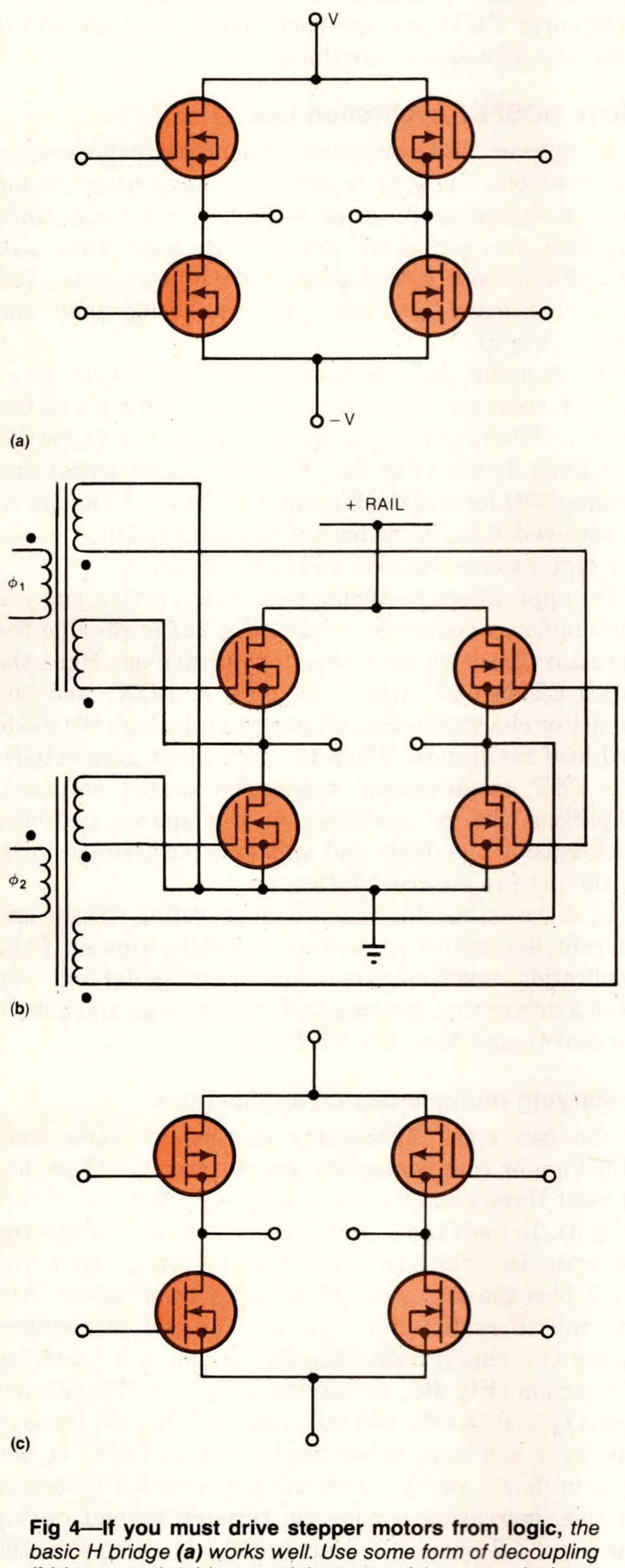


Fig 4—If you must drive stepper motors from logic, *the basic H bridge* ***(a)*** *works well. Use some form of decoupling* ***(b)*** *between the drivers and the gates of the upper device to ensure full turn-on. Of course, the simplest H-bridge circuit uses a mix of p- and n-channel MOSFETs* ***(c)****.*

charging current, and D_2 provides a low-impedance discharge path for Q_3's gate when the input is HIGH.

Several options can further improve switching characteristics. You can, for example, substitute a high-frequency bipolar npn transistor for Q_1 and use a Baker clamp between the logic input and base. Optionally, you can bias the totem pole to pull the lower device down to a negative supply rail, a configuration that tends to balance current flow both from and to the gate.

The H-bridge circuit **(Fig 4a)** especially suits driving stepper motors from logic. To pull the gates sufficiently higher than the respective source potential (within the gate-to-source voltage restriction) and thus ensure full turn-on, you must use either a complicated boostrap or some form of decoupling between the drivers and the gates of the upper devices. The decoupling scheme **(Fig 4b)** is by far the easier approach.

The simplest H-bridge circuit **(Fig 4c)** employs p-channel upper devices and n-channel lower stages. The configuration requires no bootstrap because you only have to pull the upper gate LOW to effect turn-on.

Unfortunately, all H-bridge circuits have one important limitation: You must ensure that both devices in either leg do not turn on simultaneously—a condition that would crowbar the power rails with catastrophic results. You can eliminate crowbar possibilities by using a driver with internal logic (such as the Si7250).

For simple retrofits into existing CMOS logic requiring substantial increase in current, a complementary

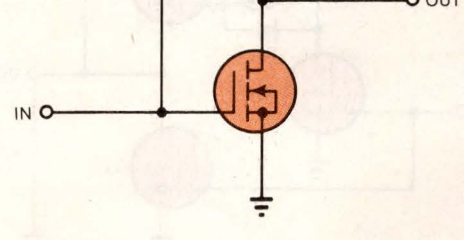


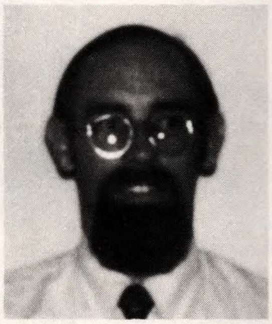
Fig 5—Although it's not the lowest cost design approach, *you can develop complementary driver circuits using MOSFETs. Because p-channel units have lower mobility and gain than n-channel FETs, you must use a larger (and more expensive) p-channel device to obtain a true complementary configuration.*

pair of power MOSFETs (**Fig 5**) offers remarkable performance. However, this benefit is not without penalties. Because the p-channel MOSFET has lower current-carrier mobility and lower gain (approximately 30%) than an n-channel unit, you must use a rather large p-channel device to obtain a true complementary circuit (defined as match of ON resistances). The result is disproportionately higher p-channel-device input capacitance and cost. Thus, you must make tradeoffs between performance and cost if you wish to use a complementary totem-pole circuit.

One word of caution concerning the use of multichip packages in totem-pole, H-bridge or complementary circuits: The maximum power-dissipation rating of the package is of prime importance. You must specify package dissipation according to the number of active elements because each device within the package contributes heat. **EDN**

Authors' biographies

Ed Oxner is a senior applications engineer in the Central Application Group at Siliconix (Santa Clara, CA), where he is responsible for the design of power systems using all the company's products. He holds a BSEE degree (with both power and communications majors) from Tri State University and is a technical advisor to ARRL and a senior member of IEEE. In addition to serving on the Editorial Review Board of *RF Design* magazine, Ed has authored numerous technical articles for a variety of trade journals and a book on the application of power FETs.



Richard Blanchard is the engineering manager of MOS-power products at Siliconix. His responsibilities include the design and development of discrete MOSpower devices and ICs utilizing MOSpower technology. Richard received his BSEE and MSEE degrees from MIT and his PhD from Stanford University. He has coauthored two books on semiconductor technology and written many articles in the areas of device physics, semiconductor technology and applications. Richard is a member of the IEEE, ECS and Sigma Xi; his leisure activities include running, hiking and woodworking.

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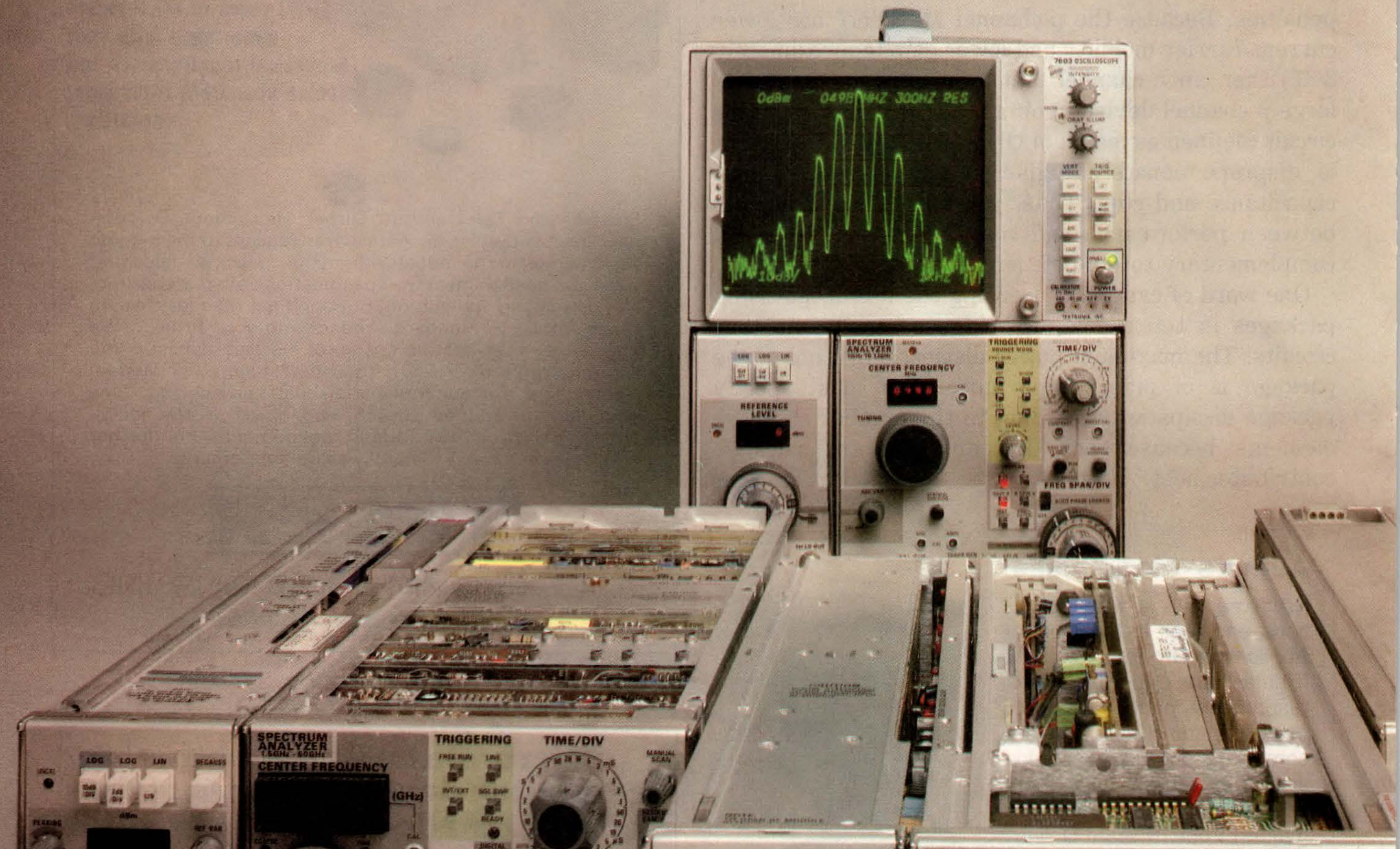

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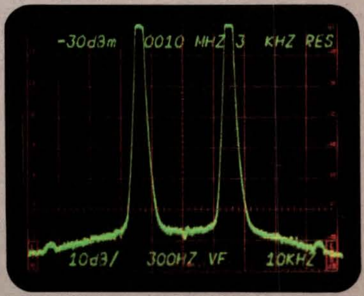

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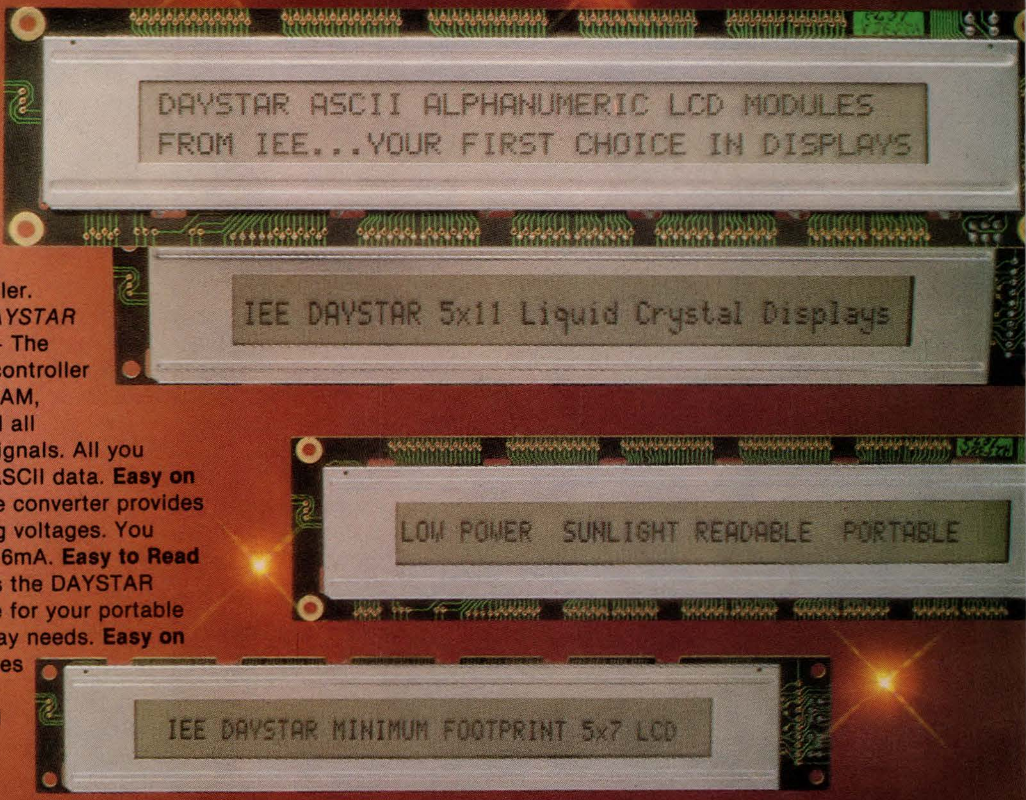

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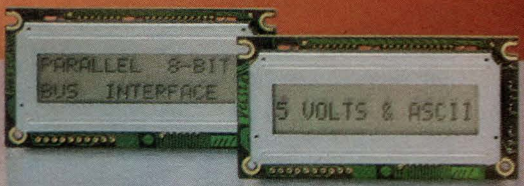

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Select precision IC op amps for optimum design performance

Confronted with an overwhelming array of precision IC op amps, you must understand the intricacies of bipolar, chopper-stabilized and FET-input types in order to best select the optimum device for your application.

Walter G Jung, Consultant

Choosing the precision IC op amp that best suits your circuit's design function requires a thorough knowledge of the performance strengths and shortcomings of available devices: Even with today's mature op-amp technology, no one device satisfies all needs.

Three different op-amp types—chopper stabilized, bipolar and FET input—compete vigorously for analog-circuit designers' attention. And despite relative technological maturity, process refinements continue to steadily improve each op-amp type's characteristics. Indeed, recent devices' performance parameters exceed those of the early 709-type units by two to three orders of magnitude in several areas.

For example, the newest FET-input op amps exhibit increased precision with regard to offset voltage and drift (EDN, November 10, pg 131). Accordingly, these devices should find favor in applications previously served by bipolar-input op amps, as well as in a range of new functions involving high-impedance elements.

This encroachment of FET-input devices into traditional bipolar territory helps emphasize the care you must take in matching units to your application requirements—as the differences among the relative merits of the three op-amp types grow more subtle, your design task becomes more complex. Moreover, be wary of data-sheet specsmanship. You must consider all op-amp parameters relative to your application's actual operating conditions and determine which factors contribute to your error budget.

Dealing with traditional op-amp problems

To demonstrate the contrasting parameters typical of precision IC op amps, consider bipolar-device offset voltage. Manufacturers can now trim this spec to within tens of microvolts. Moreover, because minimum drift occurs at offset null in a well-designed bipolar op amp, manufacturers can also hold offset-voltage drift to less than 1 μV/°C—a level sufficiently low that maintaining it during actual circuit operation requires serious consideration of external drift sources. Although bipolar op amps with trimmed offset excell in dc performance when connected to source impedances less than 100 kΩ, their approximately 1-nA bias current becomes a limiting factor when source impedances are in the megohm range.

For applications demanding less than a 1-nA bias current, FET-input op amps become attractive. They possess 10-pA or lower room-temperature bias currents, which let you connect source impedances in the hundreds of megohms. FET bias-current problems also prove insignificant for many medium-temperature applications.

FET-input devices' offset-voltage problem, however, proves worse than that of bipolar parts. Whether employing JFETs or MOSFETs, FET op amps inherently spec higher (untrimmed) offsets than do bipolar versions. Although this offset can be nulled at the wafer or board level, the resulting drift change can degrade a circuit's performance. As a result, you exchange one problem for another. Therefore, carefully examine what manufacturers designate as low-offset FET op amps. A true precision FET unit—one that simultaneously achieves low drift *and* low offset—hasn't existed until recently.

To deal effectively with these and other common problems, you must become familiar with the varied meanings the term "precision" can represent in different precision-op-amp applications. The comparison information compiled in the **table** illustrates the shortcomings and strengths of the various precision IC op-amp types.

Choppers offer low offset and drift

Based on performance, the chopper-stabilized and bipolar types have long been associated with precision applications. Indeed, chopper op amps trace their origins back to the vacuum-tube era. On the other hand, bipolar op amps have more recently attained precision status. As for FET units, they have also attained a reputation for increasing precision.

Of course, specific devices within the three categories provide both outstanding and limiting performance characteristics. For example, chopper-stabilized op amps have traditionally furnished the lowest offset voltage and drift, low bias currents and extremely high gain (150 dB or more). On the debit side, though, they give rise to commutation noise, cross modulation, open-loop-phase and overload-recovery problems, as well as requiring extra circuit components. Recent IC improvements in chopper units, such as those achieved by ICL7650 types, solve many of these problems. Still, you can't universally apply chopper op amps, although you certainly should consider them first when an application mandates stable microvolt-level offset voltages over long time periods.

Bipolar devices take on tough jobs

Based on installation experience, bipolar op amps represent the circuit designer's workhorses, starting with Model 725 and evolving through the 108/308, 504 and OP-07. On balance, they supply predictable high-performance characteristics and shine in achieving input-voltage stability relative to common-mode and power-supply variations as well as time.

However, when the application calls for picoampere-level input currents, bipolar op amps generally lose favor. This limitation occurs because they employ bias-compensated or super-beta input stages, which generally yield only about 1-nA performance. And attempts to improve this spec necessitate tradeoffs: 108/308 units, for example, achieve lower bias currents at the expense of higher voltage noise. Alternatively, OP-07 units furnish lower voltage noise but higher input currents.

Such input-stage limitations in the voltage-noise/input-current relationship extend across the spectrum of available bipolar op amps: Increasing input-stage operating current to achieve lower voltage noise can make the input bias current—and its related noise components—prohibitive. Bias-current compensation such as the scheme employed in OP-27 units helps alleviate this problem, but the noise signals, although lower in level, still remain.

Other bipolar op amps, such as the LM11, achieve lower bias currents by combining Darlington and super-beta input stages, but this technique yields higher voltage-noise levels. The LM11's bias currents are merely tens of picoamperes and stay stable despite temperature increases. For example, at 100°C, bias-current specs are still better than those of nearly all other op-amp types. (Electrometer-grade FET versions are one exception.)

As a rule, bipolar op amps exhibit slow speeds, with gain-bandwidths (f_t) ranging from 0.3 to 1 MHz and slew rates of less than 1V/μsec. However, they do have very high open-loop gains—typically greater than 120 dB—into rated 2-kΩ (min) loads. An exception are units in the low-power-drain 108/308 op-amp family, which spec lower gains into 10-kΩ (min) loads.

Use FETs for high speed

In theory, FET op amps provide several advantages over bipolar devices: very low bias and offset currents, healthy f_t ratings (generally 1 to 3 MHz) and 10V/μsec min slew rates. In addition, FET units don't incur the bias-current/noise tradeoff necessary with bipolar devices, because FETs' input current stems only from leakage. You can thus increase FETs' operating current without interaction.

In practice, however, many FET-op-amp input stages fail to realize true precision. For one thing, the initial bias current, although low at turn-on in a JFET-input op amp, rises with warmup: In fact, it doubles for each 10°C rise. Therefore, unless the FET's specification and test method permit a realistic warmup time, the data-sheet listing for bias current is questionable. To correct this problem, you must perform an educated extrapolation by accounting for the op amp's thermal resistance and power dissipation. Tricky at best, this design problem compounds when you have only typical—not worst-case—specs to work with.

On the other hand, when FETs do indeed possess precision-level bias currents, the data sheets guarantee the fact. What's more, the data sheets also define a

COMPARISON OF PRECISION IC OP-AMP TYPES

SHORTCOMINGS	STRENGTHS
CHOPPER STABILIZED	
NOISE (1/f AND CLOCK) CROSS MODULATION PHASE PROBLEMS LOW SUPPLY RANGE* EXTRA COMPONENTS REQUIRED OVERLOAD RECOVERY	VERY HIGH GAIN ULTRALOW OFFSET DRIFT ULTRALOW OFFSET LOW BIAS CURRENT HIGH COMMON-MODE REJECTION HIGH POWER-SUPPLY REJECTION
BIPOLAR	
HIGH INPUT CURRENT HIGH CURRENT NOISE LOW SPEED LOAD SENSITIVE*	LOW OFFSET LOW OFFSET DRIFT LOW BIAS CURRENT AT HIGH TEMPERATURE LOW VOLTAGE NOISE HIGH POWER-SUPPLY REJECTION HIGH COMMON-MODE REJECTION HIGH GAIN LOW POWER
FET INPUT	
HIGH OFFSET HIGH OFFSET DRIFT LOAD SENSITIVE* LOW SUPPLY RANGE* HIGH NOISE (MOSFET) HIGH BIAS CURRENT AT HIGH TEMPERATURE HIGH SUPPLY CURRENT* POOR COMMON-MODE REJECTION POOR POWER-SUPPLY REJECTION	LOW BIAS CURRENT LOW OFFSET CURRENT HIGH SPEED

*APPLIES ONLY TO SOME MODELS WITHIN THE BROAD CLASSIFICATION

warmup (maximum) limit on bias current. This current still rises with temperature, but you can now predict the worst-case condition.

Another FET type, MOSFET-input op amps in theory promise the best performance in terms of low input current. However, they require protection diodes in this case to allow safe device handling, and these diodes might reintroduce the leakage problem. Consequently, MOSFET devices can exhibit the same bias-current doubling for every 10°C temperature increase as JFETs do. For example, they exhibit 10 pA or less of input current at 25°C but 1 nA or more at 100°C. This performance limitation of both JFET and MOSFET units makes a precision bipolar unit more beneficial when the application requires high-impedance operation at more than 100°C. At 70°C or less, however, FET-type units generally excel in bias currents.

Other problems with JFET and MOSFET units center on high offset voltages and wide drifts. To combat these problems, manufacturers perform wafer trimming to reduce offset voltage to less than 1 mV in many units. But they don't normally guarantee drift below 10 μV/°C. In JFET units, no simple offset/drift relationship exists as in bipolar devices. On the contrary, offset-nulling JFET units could increase drift if the process disturbs the operating currents. MOSFET units exhibit even worse problems in this respect. Neither FET type, therefore, automatically comes with low drift. To meet this need, use a chopper-stabilized op amp or an FET type in which both offset and drift have been trimmed **(Ref 1)**.

On the plus side, JFET and MOSFET units display low current noise because of their low input currents. Voltage noise, however, proves another matter. MOSFET units show high noise levels and a very high corner frequency (1/f). Available JFET units vary in voltage noise levels, with about 15- to 40-nV/$\sqrt{\text{Hz}}$ mid-audio-range noise. Generally, available bipolar op amps are superior to JFET and MOSFET units in terms of voltage noise. **EDN**

Author's biography

Walter G Jung is a technical consultant. A prolific author, he has published eight books on IC applications. A member of the IEEE and a Fellow of the Audio Engineering Society, Walt lists music and audio engineering as his interests.

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EDN's December 17 issue is our 16th semiannual Product Showcase, an invaluable compendium of information on the most noteworthy new-product introductions of the past 6 months. You won't want to be without this fact-filled reference issue, which is organized into seven key product areas:

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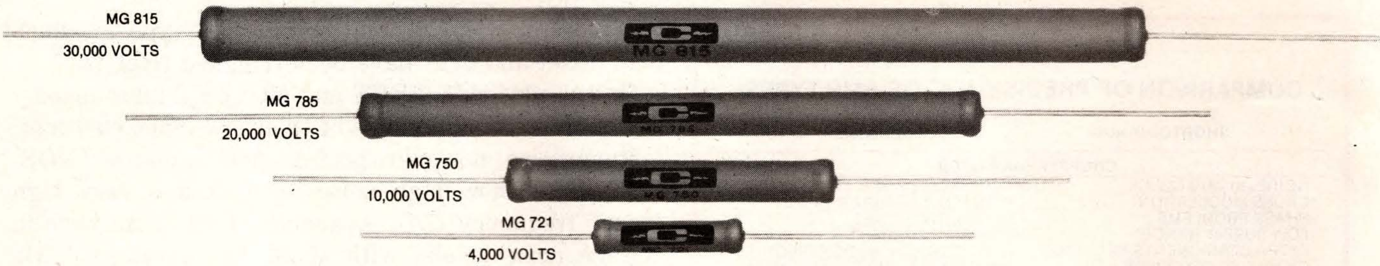
- Computers and peripherals
- ICs and semiconductors
- Instruments
- Power sources
- Products from Europe
- Software

EDN: Everything Designers Need

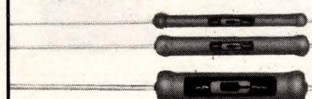
Type MG Precision High Voltage Resistors from CADDOCK deliver 6 big advantages:



1. For maximum design flexibility, there are 19 standard models with 10 voltage ratings in the Type MG 'family'.

The Type MG family of high voltage resistors includes a selection of voltage ratings from 600 volts to 30,000 volts in various resistor lengths to provide maximum flexibility in the design of high voltage assemblies.

In addition to this wide range of voltage ratings, the Type MG family provides a selection of resistor diameters at many of the standard voltage ratings, as illustrated by the three models of 4,000 volt, 1-inch long resistors shown here.



Important performance specifications for all Type MG resistors include:

- Full power rating to + 125°C.
- + 225°C maximum operating temperature.
- Resistance values that cover the range from 200 ohms to 2000 Megohms.

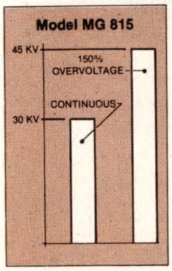
2. The standard TC of 80 PPM/°C and resistance tolerances from 1.0 % to 0.1% combine to improve circuit accuracy.

Through the full range of resistance values from 200 ohms to 2000 Megohms, the Type MG resistors maintain a temperature coefficient of 80 PPM/°C over the range from − 15°C to + 105°C, referenced to + 25°.

The combination of precision and low TC achieves a significant improvement over other high voltage resistor technologies, particularly in the higher resistance values.

3. Overvoltage rating of 150% is standard for all models.

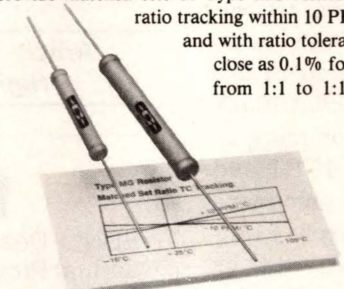
Every model of the Type MG resistors has a *standard* overvoltage/overload rating of 1.5 times the maximum working voltage where this level does not exceed 5 times the rated power. As an example, in the Model MG 815 this capability provides for short-term overloads as high as 45,000 volts.



And for even tougher applications, special factory conditioning can boost the maximum *continuous* operating voltage of many models to 160% above the standard specifications.

4. Matched resistor sets with 0.1% ratio tolerances and TC tracking as close as 10 PPM/°C from -15°C to +105°C.

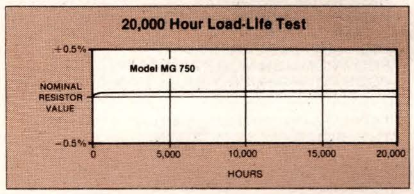
The temperature coefficient of Caddock Micronox® resistance films can be controlled to provide matched sets of Type MG resistors with ratio tracking within 10 PPM/°C and with ratio tolerances as close as 0.1% for ratios from 1:1 to 1:100,000.



For high voltage divider applications, 2% ratio tolerance is standard.

5. Extended-life stability that is typically better than 0.02% per 1000 hours.

20,000 hour *continuous* load-life tests have proven the exceptional stability of Caddock Micronox® resistance films. This graph illustrating the 20,000 hour test results of the 10,000 volt rated Model MG 750 shows extended-life stability well within 0.02% per 1000 hours.



A complete data summary of these test results is available on request.

6. Exclusive Non-Inductive Performance.

Caddock's Exclusive Non-Inductive Design is the answer wherever there are special requirements for excellent high-voltage pulse fidelity and wide bandwidths.

To keep the inductance to an absolute minimum, the special serpentine pattern provides for neighboring lines to carry the current in opposite directions to achieve maximum cancellation of flux fields over the entire length of the resistor.

Caddock's advanced film resistor technologies are the source of these exceptional performance advantages—
Produced with a special dedication to quality and unit-to-unit consistancy, these high performance film resistors have achieved an unsurpassed 20-year record of 'in-circuit' reliability.

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CIRCLE NO 52

Increase I/O-handling options with a software serial I/O port

A single-chip μC's built-in serial port can limit your options in I/O handling. You can implement a more versatile port in software, however, and get the capabilities you need from a simpler (and less expensive) chip.

Cosma Pabouctsidis, Motorola Inc

When your design requires a single-chip μC and serial I/O, you can implement a serial port in software to provide exactly the I/O features your application demands. Moreover, this software technique opens up the choice of μCs to include devices that are less expensive and perhaps better matched to your overall requirements than are off-the-shelf single-chip μCs with built-in ports. Following one such software-implementation approach can help you effectively create your own software ports.

Software overcomes hardware limitations

Indeed, adapting the scheme to your needs can help you eliminate the shortcomings of μC-resident hardware ports: A built-in port might limit you to a fixed baud rate, for instance, or else give you a choice of rates but not allow different rates for transmitting and receiving. Often, restrictions on word size and parity cause problems. Software ports have none of these limitations—changing a port's operating characteristics is as simple as changing a few lines of code.

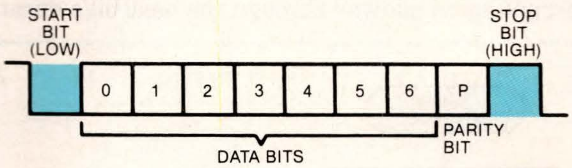


Fig 1—A serially transmitted character *begins with a LOW start bit and ends with a HIGH stop bit. In between are the data bits and a parity bit.*

A software port can also closely mimic a hardware port. The port described in this article, for example, is actually an interrupt routine and thus operates independently of other program activity once it's activated. It actually appears to the user as a hardwired device (a standard UART) with a Transmit-Data register, a Receive-Data register, a Transmit-Register-Empty flag and a Receive-Register-Full flag.

To implement a software port successfully, though, you need a good understanding of what the port must accomplish. It must handle input and output simultaneously, for example, and it must respond to input characters that arrive asynchronously. Moreover, it must handle the timing and sequencing of characters' data- and control-bit transmission and reception.

A timing diagram for a typical serial character (also called a word) appears in **Fig 1.** The word starts with a LOW-level bit (the start bit) that synchronizes the UART bit counter in a hardware port or performs a corresponding action in a software port. Data bits, a parity bit and a HIGH-level stop bit then follow. The numbers of start bits, stop bits and data bits vary among applications, and even or odd parity can apply.

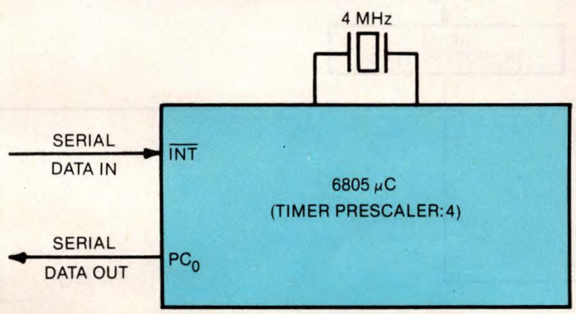


Fig 2—Using a software-based port-implementation scheme, *this 6805 μC receives serial data on its interrupt line and sends data out on line 0 (PC_0) of port C. The 4-MHz clock and divide-by-4 prescaling give the on-board timer a unit interval of 4 μsec.*

Fig 2 shows the connections that allow implementation of a software serial port in a 6805 μC. The 6805

Get the I/O features you need with a simpler and cheaper chip

receives serial data on its interrupt line and sends out data via bit 0 of port C, a 4-bit parallel port. A μC-resident timer, dedicated exclusively to the serial-I/O process, controls the intervals between individual character bits; it informs the software I/O routine, via interrupts, whenever an output bit must be sent or an input bit accepted.

The serial-input process begins when the leading edge of an input character's start bit generates an interrupt via a ONE-to-ZERO transition on the 6805's external $\overline{\text{INT}}$ line. The software's External-Interrupt routine responds to this signal by presetting the timer with a countdown value that causes the timer to reach zero—and thus generate another interrupt—midway through the start bit's duration. The software handler for this second interrupt and succeeding interrupts—the Timer-Interrupt routine—instructs the timer to interrupt again midway through the next bit's duration

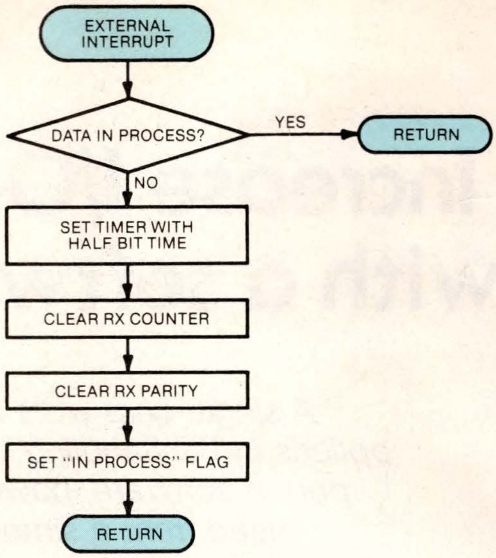
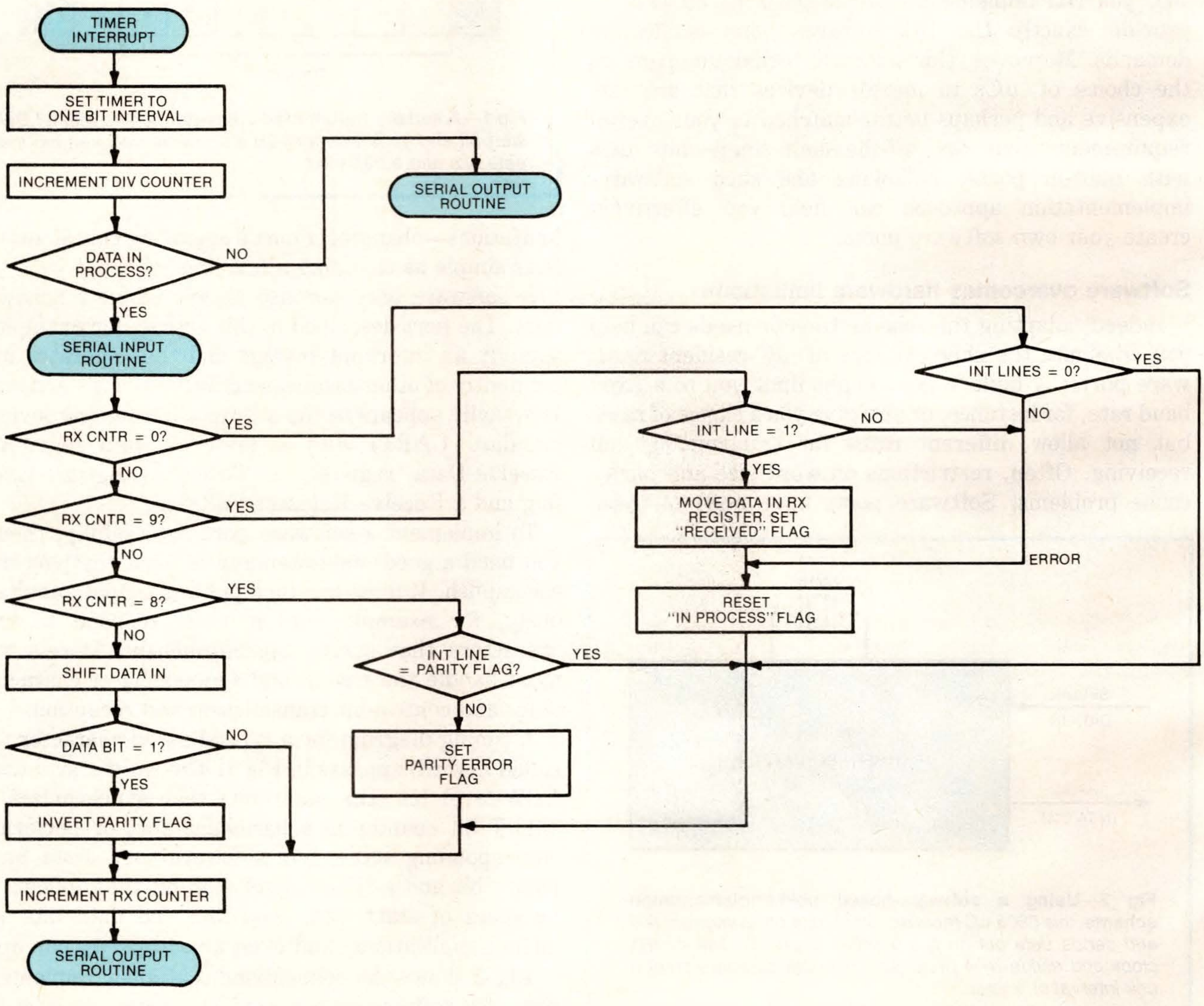


Fig 3—The External-Interrupt routine *responds to ONE-to-ZERO transitions on* $\overline{\text{INT}}$*. The routine prepares for serial input when the interrupt results from a start bit, but it ignores interrupts that result from data-bit transitions.*



until all the input word's data bits and control bits have been processed. Flowcharts for the External-Interrupt and Timer-Interrupt routines appear in **Figs 3** and **4,** respectively. This particular implementation provides 1200-baud input and 75-baud output, the rates most commonly used in videotex applications.

The preset values that the timer uses to generate interrupts depend on the chosen baud rate, interrupt response time, μC clock frequency and μC timer prescaling. If the data rate is 1200 baud, for example, the time between bits is 833 μsec, and the time from the leading edge of the start bit to the middle of the start bit is half this value, or 417 μsec. This latter value requires adjustment for the interrupt-response time, however, which is 28 μsec for this example. The timer thus requires presetting to 389 μsec. **Fig 2** shows a 4-MHz clock (resulting in a 1-μsec machine cycle) and divide-by-4 prescaling, so the timer's unit interval is 4 μsec, and the required timer preset value is 97 (or 389÷4). Because each input bit's time interval is fairly long, a timer value that's reasonably close to the calculated value (100, say) is satisfactory.

Other timer values permit different baud rates. No lower baud-rate limit exists, and the upper limit depends on the interrupt routines' execution times and extends to 4800 baud.

All serial input and output control comes from the interrupt routines **(Figs 3 and 4).** Code for the routines, written in 6805 assembly language, appears in **Fig 5.**

When an external interrupt occurs, the External-Interrupt routine checks a Receive-Data-in-Progress flag to determine if the interrupt resulted from a start bit (flag clear) or a ONE-to-ZERO transition in the input data stream (flag set). (Initialization of flags and counters occurs in the main program before any

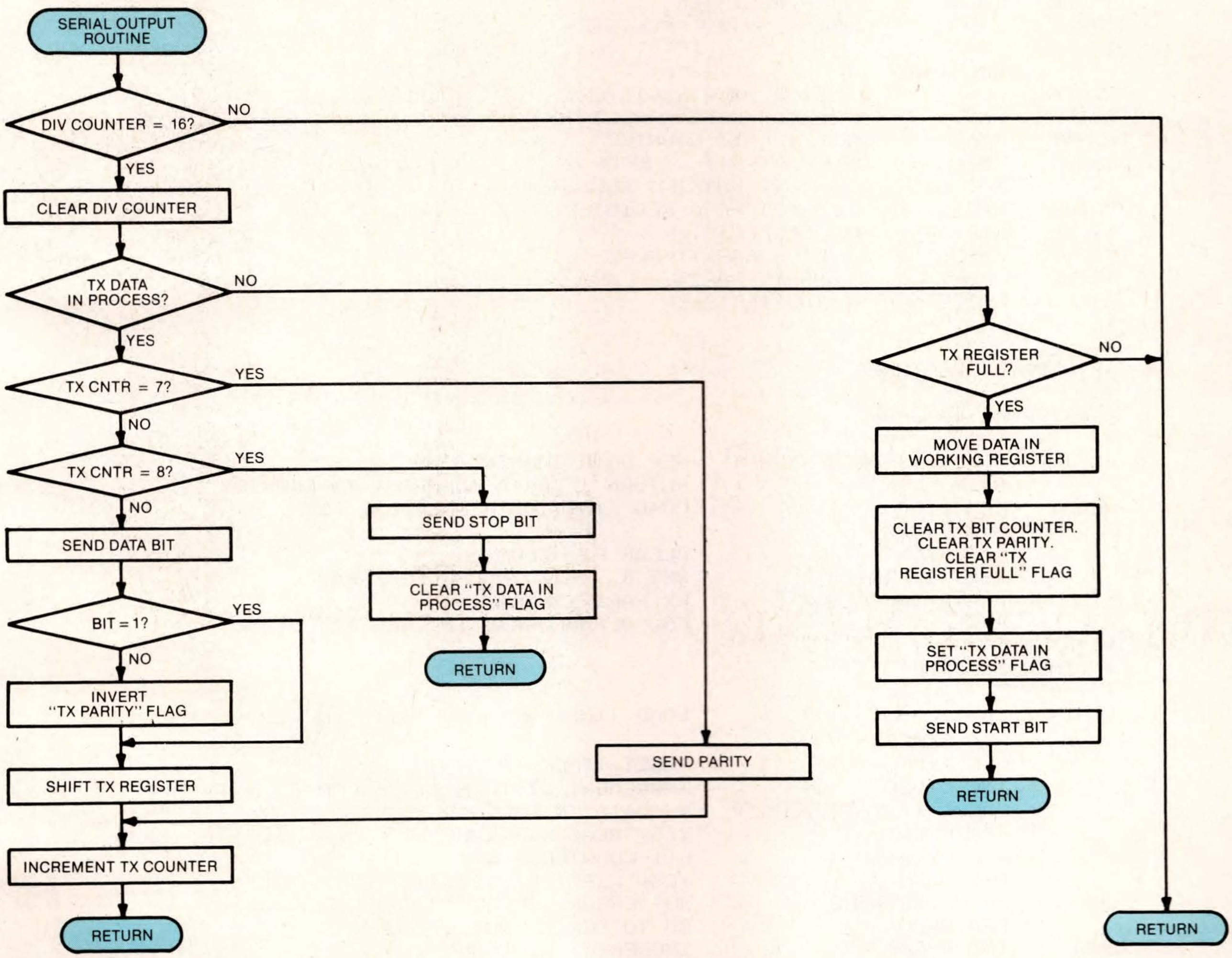


Fig 4—The Timer-Interrupt routine *controls the rates of serial input and output. In this example, the input rate is 1200 baud and the output rate is 75 baud.*

A software serial I/O port closely mimics a hardware port

interrupts.) If the routine finds the flag set, it ignores the interrupt and returns to the main program. Otherwise, the routine sets the flag to indicate a new receive sequence and clears a Receive-Bit counter and a Receive-Parity flag. As noted previously, the routine also sets the timer to trigger an interrupt midway through the start bit.

On occurrence of this timer interrupt, the Timer-Interrupt routine, which includes Serial-Input and -Output routines, first sets the timer to generate another interrupt midway through the duration of the following bit. A 1200-baud input rate, for example, thus results in 1200 timer interrupts per second during continuous data reception. The routine also maintains a counter that enables scheduling the transmission of one output character for a given number of received input

```
*
* SERIAL INPUT OUTPUT PORT BY SOFTWARE
* 1200 BAUDS RECEIVE, 75 BAUDS TRANSMIT
* 7 BITS, EVEN PARITY
*
* TABLE AND VARIABLES
*
PA      EQU 0       I/O PORTS DATA REGISTERS
PB      EQU 1
PC      EQU 2
PAD     EQU 4       I/O DATA DIRECTION REGISTERS
PBD     EQU 5
PCD     EQU 6
TIMER   EQU 8       TIMER REGISTER
TIMRG   EQU 9       TIMER CONTROL REGISTER
*
        ORG $40
RXDTA   RMB 1       RECEIVE DATA REGISTER
RXWRK   RMB 1       RECEIVE WORKING REGISTER
RXCNT   RMB 1       RECEIVE BIT COUNTER
TXCNT   RMB 1       TRANSMIT BIT COUNTER
TXWRK   RMB 1       TRANSMIT WORKING REGISTER
TXDTA   RMB 1       TRANSMIT DATA REGISTER
DIVID   RMB 1       DIVIDE REGISTER
RXPAR   RMB 1       RECEIVE PARITY FLAG
TXPAR   RMB 1       TRANSMIT PARITY FLAG
STATUS  RMB 1       STATUS REGISTER
*
*
* INTERUPT ROUTINES
*
* EXTERNAL INTERUPT
*
EXTINT  BRCLR 1,STATUS,NEWRT  NEW DATA COMMING
        RTI                   RETURN IF DATA ALLREADY IN PROCESS
NEWRT   LDA #100              LOAD TIMER WITH HALF BIT TIME
        STA TIMER
        CLR RXCNT             CLEAR BIT COUNTER
        BSET 1,STATUS         SET RX DATA IN PROCESS FLAG
        CLR RXPAR CLEAR       RX PARITY FLAG
        RTI                   END OF HARDWARE INTERRUPT ROUTINE
*
* TIMER INTERUPT
*
TIMINT  LDA #204              LOAD TIMER WITH ONE BIT TIME
        STA TIMER
        CLR TIMRG             RESET TIMER INTERRUPT
        INC DIVID             INCREMENT DIVIDER BY 16 FOR 75 BAUDS
        BRCLR 1,STATUS,SEOUT  RX DATA IN PROCESS ?
        LDA RXCNT             YES, READ BIT COUNTER
        BNE OVSA              BIT COUNTER = 0 ?
        BIL OVSB              YES, FIRST BIT ( START BIT ) =0?
ERA     BCLR 1,STATUS         NO, ERROR, CLEAR IN PROCESS FLAG
        BRA SEOUT             GO TO SERIAL OUTPUT ROUTINE
OVSB    INC RXCNT             INCREMENT RX COUNTER
```

Fig 5—Less than 150 bytes of storage *hold this software implementation of a serial I/O port. The 6805 μC's bit-manipulating instructions, such as BSET, BCLR, BRSET and BRCLR, help minimize the storage.*

characters. For the particular example in this article (1200-baud input and 75-baud output), the routine keeps a divide-by-16 counter and allows transmission of one output character for every 16 input characters.

After setting the timer and incrementing the counter, the Timer-Interrupt routine checks the Receive-Data-in-Progress flag; if it finds the flag set, it passes control to the Serial-Input routine.

The Serial-Input routine accepts one input bit each time it executes (unless an error condition arises) and converts each series of data bits and control bits to an input character. Because the bits appear on the µC's interrupt line, it's necessary to read the line's level. The 6805 has two instructions for this function: BIH (Branch if Interrupt HIGH) and BIL (Branch if Interrupt LOW). If you use a µC without such

```
        BRA SEOUT               GO TO SERIAL OUTPUT
OVSA    CMPA #$09               BIT COUNTER = 9
        BNE OVSC
        BIL ERA                 YES, STOP BIT, CHECK INPUT HIGH
        LDA RXWRK               WORD RECEIVED, MOVE DATA
        STA RXDTA               IN RECEIVE DATA REGISTER
        BSET 7,STATUS           SET RECEIVE REGISTER FULL FLAG
        BRA ERA                 GO TO SERIAL OUTPUT
OVSC    CMP #$08                BIT COUNTER = 8 ?
        BNE OVSD
        LSR RXWRK               YES, CHECK PARITY
        BRSET 0,RXPAR,PLOII
        BIH ERBB                COMPARE INPUT WITH COMPUTED PARITY
        BRA OVSB                EQUAL, GO TO SERIAL OUTPUT ROUTINE
PLOII   BIH OVSB
ERBB    BSET 7,RXWRK            PARITY ERROR, SET BIT 7 OF DATA WORD
        BRA OVSB
OVSD    LSR RXWRK               COUNTER = 1 TO 7, SHIFT IN
        BIL OVSB
        BSET 7,RXWRK            DATA BIT = 1
        COM RXPAR               YES, INVERT PARITY FLAG
        BRA OVSB                GO TO SERIAL INPUT ROUTINE
*
* SERIAL OUTPUT
*
SEOUT   LDA DIVID
        BIT #$0F                DIVIDE COUNTER = 16
        BEQ SEND                YES, PROCESS ONE OUFUT BIT
        RTI                     NO, RETURN
SEND    BRSET 3,STATUS,SENDA    TX DATA IN PROCESS ?
        BRSET 4,STATUS,NWDTA    NO, NEW DATA READY ?
        RTI                     NO, RETURN
NWDTA   LDA TXDTA
        STA TXWRK               MOVE DATA INTO WORKING REGISTER
        BSET 3,STATUS           SET DATA IN PROCESS FLAG
        BCLR 4,STATUS           CLEAR TX REGISTER FULL FLAG
        CLR TXCNT               CLEAR OUTPUT BIT COUNTER
        CLR TXPAR               CLEAR TXMIT PARITY COUNTER
        BCLR 0,PC               SEND START BIT
        RTI
SENDA   LDA TXCNT               READ TXMIT BIT COUNTER
        CMP #$07                COUNTER = 7
        BNE SENDC
        LDA TXPAR               YES, SEND PARITY BIT
        STA TXWRK
SENDC   BRCLR 3,TXCNT,SENDB     BIT COUNTER = 8 ?
        BSET 0,PC               YES, ALL BITS SENT, SEND STOP BIT
        BCLR 3,STATUS           CLEAR TX DATA IN PROCESS FLAG
        RTI
SENDB   BRSET 0,TXWRK,ONE       SEND DATA BITS, ONE OR ZERO
        BCLR 0,PC               SEND ZERO
        BRA OVRRA
ONE     BSET 0,PC               SEND ONE
        COM TXPAR               INVERT PARITY FLAG
OVRRA   ASR TXWRK               SHIFT WORKING REGISTER
        INC TXCNT               INCREMENT BIT COUNTER
        RTI
        END
```

The software port appears to the user as a standard UART

instructions, you need to bring the serial data in on a normal input pin and read it with standard input instructions.

The Serial-Input routine needs to know which bit to expect at any given time, so it keeps tabs on the bits with the Receive-Bit counter. If the Receive-Bit count is 0, the input bit is a start bit and should be LOW. If the count is 8, the input bit is the parity bit, which gets compared with a program-generated Parity flag. A mismatch of the parity bit and the Parity flag causes the routine to set a Parity-Error flag. For a bit count of 9, the routine expects a stop bit (input HIGH), indicating that the word is complete.

For counter values from 1 through 7, the input bit is a normal data bit, which the routine shifts into a working register. The routine also inverts the Parity flag each time the received data bit is a ONE. After receiving all the bits of a word, the routine moves the word from a working register to the Receive-Data register and sets the Receive-Register-Full flag to inform the main program that a new data word is available.

Output routine transmits at different rate

After the reception and processing of each input data bit, or at each timer interrupt if no input data exists, control passes to the Serial-Output routine. This routine then checks the divide-by-16 counter (maintained by the Timer-Interrupt routine) to determine if it's time to transmit a data bit or control bit. If it's not yet time, the routine returns to the main program; otherwise, the routine clears the counter and prepares to transmit.

Before proceeding, the routine checks a Transmit-Data-in-Progress flag to determine if a character transmission is already underway. If a transmission isn't underway, the routine checks to see if the main program is requesting a transmission. The main program makes such a request by setting the Transmit-Register-Full flag, indicating that an output data word is in the Transmit-Data register. If the main program isn't making a request, the routine relinquishes control with a return statement.

If the main program has requested a transmission, the Serial-Output routine moves the output word from the Transmit-Data register into a working register. It then initializes a Transmit-Bit counter to 0 and clears the Transmit-Parity and Transmit-Register-Full flags. This last action informs the main program that it can load the next output character (if any) into the Transmit-Data register. Finally, the output routine sets the Transmit-Data-in-Progress flag, sends a start bit (a ZERO) and returns to the main program.

If the Serial-Output routine finds that a character transmission is already underway, however, it continues that transmission. Because it needs to know which bit of a word it's currently working on, the routine maintains a Transmit-Bit counter.

```
* OUTPUT ONE CHARACTER
OUTCH   BRSET 4,STATUS,OUTCH   WAIT UNTIL TXMIT REGISTER EMPTY
        STA TXDTA
(a)     BSET 4,STATUS          SET TX REGISTER FULL FLAG

* INPUT ONE CHARACTER
INCH    BRCLR 7,STATUS,INCH    WAIT UNTIL RECEIVE REGISTER FULL
        LDA RXDTA              READ DATA
(b)     BCLR 7,STATUS          CLEAR REGISTER FULL FLAG
```

Fig 6—Only three lines of code *are required to initiate transmission* ***(a)*** *or reception* ***(b)*** *of a serial character.*

When the output routine finds a Transmit-Bit counter value between 0 and 6, it sends a data bit by moving the working register's least significant bit to the output port and then shifts the register contents right one bit. It also increments the Transmit-Bit counter, and it inverts the Transmit-Parity flag if the transmitted data bit is a ONE.

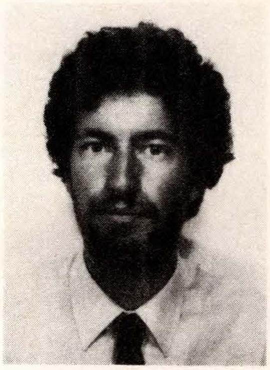
When the bit count is 7, the routine puts its internally generated parity bit on the output line and then increments the Transmit-Bit counter. For a bit count of 8, the routine sends a stop bit (a ONE) and clears the Transmit-Data-in-Progress flag, indicating that the transmission is complete.

You use the software serial I/O port much as you would use a hardwired UART. To transmit a character **(Fig 6a)**, wait until the Transmit-Register-Full flag is clear and then store the character in the Transmit-Data register and set the Transmit-Register-Full flag. To accept an input character **(Fig 6b)**, wait until the Receive-Register-Full flag is set and then read the Receive-Data register and clear the Receive-Register-Full flag.

Although it isn't done in this example, you can also simulate a UART's additional control lines, such as a Clear-to-Send line and a Carrier-Detect line, on a μC's standard I/O pins. With some additional effort, you can also extend the example approach to a dual serial port or automatic baud-rate setting. **EDN**

Author's biography

Cosma Pabouctsidis is a system engineer with Motorola's European Semiconductor Div (Geneva, Switzerland). He holds a BSEE equivalent from Ecole Technique Superieure of Geneva, and his work responsibilities include defining new ICs for telecomm applications. In his spare time, Cosma enjoys video, personal computers, sailing and skiing.



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Use a programmable calculator to ease transformer design

Two TI-59 programs can significantly reduce the time required to design efficient transformers. One determines such parameters as turns ratio and copper loss; the other provides a preliminary design evaluation.

Gerald West, Honeywell

Written for the TI-59 programmable calculator, the two programs described here can help you develop push/pull switching or power-coupling transformers, reducing design time from hours or days to minutes. One program **(Table 1)** lets you enter core data and transformer operating requirements into the calculator, which then provides the basic fabrication information. To complete the design cycle, you can then use the other program **(Table 2)** to test the transformer developed by the design program.

Program computing tools

Before looking at program operation, consider the theory behind the calculator algorithms. Essentially, the programs use seven equations to generate a complete transformer design. For a push/pull switching transformer, the program calculates an initial turns ratio A using the expression

$$A = \frac{\sqrt{2}\,\pi\, V_{OUT}}{8V_{CC}},$$

where V_{OUT} is the rms output voltage and V_{CC} is the dc source voltage. If the design problem involves an isolation power transformer, the program uses the I/O voltage ratio to calculate the initial turns ratio.

Faraday's Law determines the secondary turns:

$$N = \frac{V_{OUT}}{BA_E fk \times 10^{-8}},$$

where N=number of turns, B=flux density (G), A_E=effective core area (cm^2), f=frequency (Hz) and k=4.44 (for a power transformer) or 4.0 (for a switching transformer). The expression

$$L_P = A_L(N_P)^2,$$

where L_P is the primary inductance (H), A_L is the inductance constant (H/N^2) and N_P is the number of primary turns, calculates the primary inductance with the secondary open-circuited.

To determine wire size, the program uses

$$CM_S = \left[\frac{A_W(FIL)}{2N_S(100)(2.54)^2}\right]$$

and

$$CM_P = \frac{1}{N_P}\left[\frac{A_W(FIL)}{100(2.54)^2} - N_S(CM_S \times 10^{-6})\right],$$

where A_W equals window area (cm^2) and FIL is the fill factor (%), to calculate total conductor-area requirements in circular mils (CM) for the secondary (cm_S) and primary (cm_P) windings, respectively.

After the program determines the circular-mil area for secondary and primary windings, it calculates the nearest wire gauge required:

$$AWG = 36 - \left[\frac{39}{\log 92}\left(\log(DIA) - \log 0.005\right)\right],$$

where

$$DIA = \sqrt{CM \times 10^{-6}}.$$

Conversely, the specific wire diameter for the wire gauge selected equals

$$W_D = 0.005\left(\sqrt[39]{92}\right)^{36-AWG},$$

Transformer design program offers dramatic time savings

where W_D is measured in inches. This figure is used for program calculation of copper loss. (The program uses a 20°C value of 1.7241×10^{-6} Ωcm for copper resistivity.)

Design-program overview

Using these equations, the design program calculates primary and secondary turns, primary and secondary wire gauge, turns ratio (secondary/full primary), primary- and secondary-winding current density, primary inductance (with open-circuit secondary) and copper loss. You can enter core loss in watts (obtained by referring to specific core-loss information, often expressed in terms of watts per unit weight or per unit volume as a function of frequency and flux density) by pressing the calculator's SBR and EE keys, which allows it to record the core loss spec for comparison against the calculated copper loss. (Note that maximizing transformer efficiency usually requires that the copper loss equal the core loss. This condition usually occurs when current density is about 300A/cm² and when the core operates below saturation. The program presented here allows you to evaluate in as short a time as 30 sec whether such conditions are met.) Finally, the program calculates and records transformation efficiency for a unity-power-factor load.

Before you key-in the program, you must press 3, OP and 17 (the calculator then displays 719.29) to partition the calculator for 720 program-step and 30 memory registers. After loading the program, enter all transformer operating specs (such as source voltage, VA rating, frequency and selected flux level) using the second-function user-defined keys A′ through E′. User-defined keys A through E serve for direct entry of core parameters such as inductance constant, core area and window area as well as mean turn length and fill factor for the transformer windings within the window. (The program uses only bare-copper dimensions in the calculations—thus allowing some design leeway concerning the insulation thickness, amount of insulation wrapping and fill factor.)

To execute the program, press the SBR and = keys. The printer indicates PWR (power-coupling transformer) or SW (push/pull switching transformer) at the beginning of each calculation run. To select the switching-transformer design, set Flag 1 before pressing SBR =. The program rounds off number of turns and wire gauges. **Table 3** illustrates the printer output.

Designing by the numbers

A design example—for a switching transformer that must deliver 0.25A rms/400V rms at 30-kHz fundamental switching frequency—illustrates program capability and operation. The push/pull switching transistors will operate from a 100V dc source, and you'll need a core material that can operate below saturation at 1500G.

For this example, assume that a catalog search yields a pot core with an 8.3×10^{-6}-H/N² inductance constant, 1.38-cm² core area, 0.587-cm² window area and 6.2-cm mean turn length. Proceed as follows:

1. Enter dc voltage V_{CC}, press A′ and set Flag 1. (This last step, which you accomplish by pressing the 2nd, St Flg and 1 keys, selects the push/pull switching-transformer option.)

2. Enter rms output voltage V_{OUT} and press B′.

3. Enter rms output current I_{OUT} and press C′.

4. Enter operating frequency (in Hz) and press D′.

TABLE 1—DESIGN-PROGRAM LISTING

000	76	LBL	025	05	05	050	10	10	075	07	7	100	07	7	125	04	4	150	06	06
001	11	A	026	91	R/S	051	91	R/S	076	00	0	101	03	3	126	02	2	151	02	2
002	42	STO	027	76	LBL	052	76	LBL	077	69	OP	102	05	5	127	02	2	152	04	4
003	01	01	028	16	A'	053	95	=	078	04	04	103	03	3	128	04	4	153	03	3
004	22	INV	029	42	STO	054	01	1	079	43	RCL	104	01	1	129	03	3	154	02	2
005	52	EE	030	06	06	055	03	3	080	02	02	105	69	OP	130	01	1	155	04	4
006	91	R/S	031	91	R/S	056	02	2	081	69	OP	106	04	04	131	69	OP	156	01	1
007	76	LBL	032	76	LBL	057	07	7	082	06	06	107	43	RCL	132	04	04	157	03	3
008	12	B	033	17	B'	058	69	OP	083	04	4	108	04	04	133	43	RCL	158	07	7
009	42	STO	034	42	STO	059	04	04	084	03	3	109	69	OP	134	06	06	159	69	OP
010	02	02	035	07	07	060	43	RCL	085	01	1	110	06	06	135	69	OP	160	04	04
011	91	R/S	036	91	R/S	061	01	01	086	05	5	111	06	6	136	06	06	161	43	RCL
012	76	LBL	037	76	LBL	062	57	ENG	087	03	3	112	01	1	137	04	4	162	08	08
013	13	C	038	18	C'	063	69	OP	088	00	0	113	02	2	138	02	2	163	69	OP
014	42	STO	039	42	STO	064	06	06	089	07	7	114	01	1	139	03	3	164	06	06
015	03	03	040	08	08	065	22	INV	090	00	0	115	02	2	140	02	2	165	02	2
016	91	R/S	041	91	R/S	066	57	ENG	091	69	OP	116	04	4	141	04	4	166	03	3
017	76	LBL	042	76	LBL	067	22	INV	092	04	04	117	02	2	142	01	1	167	04	4
018	14	D	043	19	D'	068	52	EE	093	43	RCL	118	07	7	143	03	3	168	06	6
019	42	STO	044	42	STO	069	01	1	094	03	03	119	69	OP	144	07	7	169	69	OP
020	04	04	045	09	09	070	05	5	095	69	OP	120	04	04	145	69	OP	170	04	04
021	91	R/S	046	91	R/S	071	01	1	096	06	06	121	43	RCL	146	04	04	171	43	RCL
022	76	LBL	047	76	LBL	072	05	5	097	03	3	122	05	05	147	43	RCL	172	09	09
023	15	E	048	10	E'	073	03	3	098	00	0	123	69	OP	148	07	07	173	69	OP
024	42	STO	049	42	STO	074	00	0	099	03	3	124	06	06	149	69	OP	174	06	06

175	02	2
176	02	2
177	01	1
178	03	3
179	04	4
180	01	1
181	03	3
182	06	6
183	69	OP
184	04	04
185	43	RCL
186	10	10
187	69	OP
188	06	06
189	98	ADV
190	87	IFF
191	01	01
192	78	Σ+
193	69	OP
194	00	00
195	03	3
196	03	3
197	04	4
198	03	3
199	03	3
200	05	5
201	69	OP
202	01	01
203	69	OP
204	05	05
205	43	RCL
206	07	07
207	55	÷
208	43	RCL
209	06	06
210	95	=
211	42	STO
212	11	11
213	43	RCL
214	07	07
215	55	÷
216	43	RCL
217	10	10
218	55	÷
219	43	RCL
220	02	02
221	55	÷
222	43	RCL
223	09	09
224	55	÷
225	04	4
226	93	.
227	04	4
228	04	4
229	52	EE
230	94	+/-
231	08	8
232	95	=
233	61	GTO
234	79	$\bar{x}$
235	76	LBL
236	78	Σ+
237	69	OP
238	00	00
239	03	3
240	06	6
241	04	4
242	03	3
243	69	OP
244	01	01
245	69	OP
246	05	05
247	43	RCL
248	07	07
249	65	×
250	89	π
251	65	×
252	02	2
253	34	$\sqrt{x}$
254	55	÷
255	08	8
256	55	÷
257	43	RCL
258	06	06
259	95	=
260	42	STO
261	11	11

262	43	RCL
263	07	07
264	55	÷
265	43	RCL
266	10	10
267	55	÷
268	43	RCL
269	02	02
270	55	÷
271	43	RCL
272	09	09
273	55	÷
274	04	4
275	52	EE
276	94	+/-
277	08	8
278	95	=
279	76	LBL
280	79	$\bar{x}$
281	22	INV
282	52	EE
283	58	FIX
284	00	00
285	52	EE
286	22	INV
287	52	EE
288	42	STO
289	12	12
290	55	÷
291	43	RCL
292	11	11
293	95	=
294	52	EE
295	22	INV
296	52	EE
297	42	STO
298	13	13
299	22	INV
300	58	FIX
301	43	RCL
302	03	03
303	65	×
304	43	RCL
305	05	05
306	55	÷
307	01	1
308	00	0
309	00	0
310	55	÷
311	02	2
312	55	÷
313	43	RCL
314	12	12
315	95	=
316	42	STO
317	14	14
318	55	÷
319	02	2
320	93	.
321	05	5
322	04	4
323	33	X^2
324	95	=
325	34	$\sqrt{x}$
326	95	=
327	42	STO
328	15	15
329	42	STO
330	29	29
331	71	SBR
332	42	STO
333	42	STO
334	16	16
335	22	INV
336	58	FIX
337	53	(
338	43	RCL
339	03	03
340	65	×
341	43	RCL
342	05	05
343	55	÷
344	01	1
345	00	0
346	00	0
347	75	-

348	43	RCL
349	14	14
350	65	×
351	43	RCL
352	12	12
353	54	)
354	55	÷
355	43	RCL
356	13	13
357	95	=
358	42	STO
359	17	17
360	55	÷
361	02	2
362	93	.
363	05	5
364	04	4
365	33	X^2
366	95	=
367	34	$\sqrt{x}$
368	95	=
369	42	STO
370	18	18
371	42	STO
372	29	29
373	71	SBR
374	42	STO
375	42	STO
376	19	19
377	42	STO
378	29	29
379	22	INV
380	58	FIX
381	43	RCL
382	01	01
383	65	×
384	43	RCL
385	13	13
386	33	X^2
387	95	=
388	42	STO
389	20	20
390	71	SBR
391	43	RCL
392	42	STO
393	21	21
394	43	RCL
395	16	16
396	42	STO
397	29	29
398	71	SBR
399	43	RCL
400	42	STO
401	22	22
402	43	RCL
403	08	08
404	65	×
405	04	4
406	55	÷
407	53	(
408	89	π
409	65	×
410	53	(
411	43	RCL
412	22	22
413	65	×
414	02	2
415	93	.
416	05	5
417	04	4
418	54	)
419	33	X^2
420	54	)
421	95	=
422	42	STO
423	23	23
424	43	RCL
425	12	12
426	55	÷
427	43	RCL
428	13	13
429	95	=
430	42	STO
431	24	24
432	65	×
433	43	RCL

434	08	08
435	65	×
436	04	4
437	55	÷
438	89	π
439	55	÷
440	53	(
441	53	(
442	43	RCL
443	21	21
444	65	×
445	02	2
446	93	.
447	05	5
448	04	4
449	54	)
450	33	X^2
451	54	)
452	95	=
453	42	STO
454	25	25
455	01	1
456	93	.
457	07	7
458	02	2
459	04	4
460	01	1
461	52	EE
462	94	+/-
463	06	6
464	65	×
465	43	RCL
466	04	04
467	65	×
468	43	RCL
469	08	08
470	33	X^2
471	65	×
472	53	(
473	43	RCL
474	12	12
475	55	÷
476	43	RCL
477	14	14
478	85	+
479	43	RCL
480	13	13
481	65	×
482	43	RCL
483	24	24
484	33	X^2
485	55	÷
486	43	RCL
487	17	17
488	54	)
489	95	=
490	42	STO
491	26	26
492	22	INV
493	52	EE
494	03	3
495	01	1
496	03	3
497	03	3
498	03	3
499	05	5
500	02	2
501	04	4
502	69	OP
503	04	04
504	43	RCL
505	13	13
506	69	OP
507	06	06
508	01	1
509	03	3
510	04	4
511	03	3
512	02	2
513	02	2
514	03	3
515	03	3
516	69	OP
517	04	04
518	43	RCL
519	19	19

520	69	OP
521	06	06
522	03	3
523	01	1
524	03	3
525	06	6
526	01	1
527	07	7
528	01	1
529	05	5
530	69	OP
531	04	04
532	43	RCL
533	12	12
534	69	OP
535	06	06
536	01	1
537	03	3
538	04	4
539	03	3
540	02	2
541	02	2
542	03	3
543	06	6
544	69	OP
545	04	04
546	43	RCL
547	16	16
548	69	OP
549	06	06
550	00	0
551	02	2
552	06	6
553	02	2
554	01	1
555	03	3
556	69	OP
557	04	04
558	43	RCL
559	24	24
560	69	OP
561	06	06
562	02	2
563	05	5
564	03	3
565	03	3
566	03	3
567	05	5
568	02	2
569	04	4
570	69	OP
571	04	04
572	43	RCL
573	25	25
574	69	OP
575	06	06
576	02	2
577	05	5
578	03	3
579	06	6
580	01	1
581	07	7
582	01	1
583	05	5
584	69	OP
585	04	04
586	43	RCL
587	23	23
588	69	OP
589	06	06
590	02	2
591	07	7
592	03	3
593	03	3
594	03	3
595	05	5
596	02	2
597	04	4
598	69	OP
599	04	04
600	43	RCL
601	20	20
602	69	OP
603	06	06
604	01	1
605	05	5

606	04	4
607	01	1
608	69	OP
609	04	04
610	43	RCL
611	26	26
612	69	OP
613	06	06
614	91	R/S
615	76	LBL
616	42	STO
617	03	3
618	06	6
619	75	-
620	03	3
621	09	9
622	65	×
623	53	(
624	43	RCL
625	29	29
626	28	LOG
627	75	-
628	93	.
629	00	0
630	00	0
631	05	5
632	28	LOG
633	54	)
634	55	÷
635	09	9
636	02	2
637	28	LOG
638	95	=
639	58	FIX
640	00	00
641	52	EE
642	22	INV
643	52	EE
644	92	RTN
645	76	LBL
646	43	RCL
647	93	.
648	00	0
649	00	0
650	05	5
651	65	×
652	53	(
653	09	9
654	02	2
655	22	INV
656	45	Y^x
657	03	3
658	09	9
659	54	)
660	45	Y^x
661	53	(
662	03	3
663	06	6
664	75	-
665	43	RCL
666	29	29
667	54	)
668	95	=
669	92	RTN
670	76	LBL
671	52	EE
672	42	STO
673	27	27
674	01	1
675	05	5
676	03	3
677	02	2
678	03	3
679	05	5
680	01	1
681	07	7
682	69	OP
683	04	04
684	43	RCL
685	27	27
686	69	OP
687	06	06
688	06	6
689	01	1
690	69	OP
691	04	04

692	43	RCL
693	07	07
694	65	×
695	43	RCL
696	08	08
697	55	÷
698	53	(
699	43	RCL
700	26	26
701	85	+
702	43	RCL
703	27	27
704	85	+
705	43	RCL
706	07	07
707	65	×
708	43	RCL
709	08	08
710	54	)
711	65	×
712	01	1
713	00	0
714	00	0
715	95	=
716	69	OP
717	06	06
718	98	ADV
719	91	R/S

001	11	A
008	12	B
013	13	C
018	14	D
023	15	E
028	16	A'
033	17	B'
038	18	C'
043	19	D'
048	10	E'
053	95	=
236	78	Σ+
280	79	$\bar{x}$
616	42	STO
646	43	RCL
671	52	EE

TABLE 2—TEST-PROGRAM LISTING

000	03	3
001	02	2
002	03	3
003	03	3
004	01	1
005	07	7
006	03	3
007	01	1
008	69	OP
009	01	01
010	01	1
011	05	5
012	02	2
013	04	4
014	03	3
015	05	5
016	01	1
017	05	5
018	69	OP
019	02	02
020	04	4
021	01	1
022	02	2
023	04	4
024	03	3
025	07	7
026	00	0
027	00	0
028	01	1
029	06	6
030	69	OP
031	03	03
032	01	1
033	03	3
034	03	3
035	07	7
036	01	1
037	03	3
038	00	0
039	00	0
040	00	0
041	00	0
042	69	OP
043	04	04
044	69	OP
045	05	05
046	01	1
047	42	STO
048	00	00
049	02	2
050	07	7
051	42	STO
052	07	07
053	01	1
054	01	1
055	42	STO
056	04	04
057	25	CLR
058	91	R/S
059	76	LBL
060	11	A
061	42	STO
062	01	01
063	01	1
064	03	3
065	03	3
066	00	0
067	03	3
068	03	3
069	03	3
070	06	6
071	69	OP
072	04	04
073	43	RCL
074	01	01
075	69	OP
076	06	06
077	22	INV
078	52	EE
079	91	R/S
080	76	LBL
081	12	B
082	42	STO
083	02	02
084	04	4
085	02	2
086	03	3
087	02	2
088	02	2
089	07	7
090	03	3
091	07	7
092	69	OP
093	04	04
094	43	RCL
095	02	02
096	69	OP
097	06	06
098	22	INV
099	52	EE
100	91	R/S
101	76	LBL
102	13	C
103	86	STF
104	02	02
105	42	STO
106	03	03
107	03	3
108	06	6
109	01	1
110	07	7
111	01	1
112	05	5
113	69	OP
114	04	04
115	43	RCL
116	03	03
117	69	OP
118	06	06
119	22	INV
120	52	EE
121	61	GTO
122	23	LNX
123	76	LBL
124	18	C'
125	86	STF
126	03	03
127	42	STO
128	06	06
129	01	1
130	06	6
131	01	1
132	07	7
133	02	2
134	02	2
135	69	OP
136	04	04
137	43	RCL
138	06	06
139	69	OP
140	06	06
141	76	LBL
142	23	LNX
143	73	RC*
144	00	00
145	72	ST*
146	04	04
147	69	OP
148	20	20
149	69	OP
150	24	24
151	73	RC*
152	00	00
153	72	ST*
154	04	04
155	69	OP
156	20	20
157	69	OP
158	24	24
159	73	RC*
160	00	00
161	72	ST*
162	04	04
163	01	1
164	42	STO
165	00	00
166	43	RCL
167	06	06
168	72	ST*
169	07	07
170	69	OP
171	27	27
172	01	1
173	04	4
174	42	STO
175	04	04
176	87	IFF
177	01	01
178	44	SUM
179	86	STF
180	01	01
181	03	3
182	06	6
183	02	2
184	03	3
185	03	3
186	02	2
187	03	3
188	05	5
189	69	OP
190	01	01
191	03	3
192	07	7
193	00	0
194	00	0
195	01	1
196	05	5
197	02	2
198	04	4
199	03	3
200	05	5
201	69	OP
202	02	02
203	01	1
204	05	5
205	04	4
206	01	1
207	02	2
208	04	4
209	03	3
210	07	7
211	00	0
212	00	0
213	69	OP
214	03	03
215	01	1
216	06	6
217	01	1
218	03	3
219	03	3
220	07	7
221	01	1
222	03	3
223	00	0
224	00	0
225	69	OP
226	04	04
227	69	OP
228	05	05
229	69	OP
230	00	00
231	25	CLR
232	91	R/S
233	76	LBL
234	44	SUM
235	69	OP
236	00	00
237	02	2
238	01	1
239	03	3
240	05	5
241	01	1
242	07	7
243	03	3
244	04	4
245	69	OP
246	01	01
247	69	OP
248	05	05
249	69	OP
250	00	00
251	25	CLR
252	91	R/S
253	76	LBL
254	14	D
255	42	STO
256	05	05
257	02	2
258	03	3
259	04	4
260	06	6
261	69	OP
262	04	04
263	43	RCL
264	05	05
265	69	OP
266	06	06
267	69	OP
268	00	00
269	03	3
270	07	7
271	04	4
272	01	1
273	03	3
274	05	5
275	03	3
276	01	1
277	69	OP
278	01	01
279	03	3
280	06	6
281	00	0
282	00	0
283	03	3
284	05	5
285	01	1
286	03	3
287	03	3
288	07	7
289	69	OP
290	02	02
291	02	2
292	04	4
293	03	3
294	02	2
295	00	0
296	00	0
297	00	0
298	00	0
299	00	0
300	00	0
301	69	OP
302	03	03
303	69	OP
304	05	05
305	69	OP
306	00	00
307	25	CLR
308	91	R/S
309	76	LBL
310	15	E
311	42	STO
312	26	26
313	01	1
314	03	3
315	69	OP
316	04	04
317	43	RCL
318	26	26
319	69	OP
320	06	06
321	91	R/S
322	76	LBL
323	95	=
324	98	ADV
325	43	RCL
326	13	13
327	65	×
328	43	RCL
329	05	05
330	65	×
331	03	3
332	06	6
333	00	0
334	95	=
335	42	STO
336	17	17
337	43	RCL
338	16	16
339	65	×
340	43	RCL
341	05	05
342	65	×
343	03	3
344	06	6
345	00	0
346	95	=
347	42	STO
348	18	18
349	87	IFF
350	02	02
351	53	(
352	43	RCL
353	27	27
354	42	STO
355	09	09
356	43	RCL
357	28	28
358	42	STO
359	10	10
360	87	IFF
361	03	03
362	54	)
363	76	LBL
364	53	(
365	43	RCL
366	17	17
367	42	STO
368	09	09
369	43	RCL
370	18	18
371	42	STO
372	10	10
373	76	LBL
374	54	)
375	03	3
376	05	5
377	03	3
378	06	6
379	69	OP
380	04	04
381	43	RCL
382	09	09
383	39	COS
384	65	×
385	43	RCL
386	12	12
387	55	÷
388	43	RCL
389	11	11
390	95	=
391	42	STO
392	20	20
393	69	OP
394	06	06
395	04	4
396	04	4
397	03	3
398	06	6
399	69	OP
400	04	04
401	43	RCL
402	09	09
403	38	SIN
404	65	×
405	43	RCL
406	12	12
407	55	÷
408	43	RCL
409	11	11
410	95	=
411	42	STO
412	21	21
413	69	OP
414	06	06
415	02	2
416	07	7
417	03	3
418	03	3
419	03	3
420	05	5
421	02	2
422	04	4
423	69	OP
424	04	04
425	43	RCL
426	12	12
427	65	×
428	43	RCL
429	09	09
430	38	SIN
431	55	÷
432	53	(
433	02	2
434	65	×
435	89	π
436	65	×
437	43	RCL
438	05	05
439	65	×
440	43	RCL
441	11	11
442	54	)
443	95	=
444	42	STO
445	22	22
446	69	OP
447	06	06
448	43	RCL
449	15	15
450	65	×
451	43	RCL
452	10	10
453	38	SIN
454	55	÷
455	53	(
456	02	2
457	65	×
458	89	π
459	65	×
460	43	RCL
461	05	05
462	65	×
463	43	RCL
464	14	14
465	54	)
466	95	=
467	42	STO
468	23	23
469	02	2
470	06	6
471	69	OP
472	04	04
473	53	(
474	01	1
475	75	-
476	43	RCL
477	23	23
478	55	÷
479	43	RCL
480	22	22
481	54	)
482	34	√X
483	42	STO
484	24	24
485	69	OP
486	06	06
487	02	2
488	07	7
489	06	6
490	05	5
491	69	OP
492	04	04
493	53	(
494	01	1
495	75	-
496	43	RCL
497	24	24
498	54	)
499	65	×
500	53	(
501	01	1
502	85	+
503	43	RCL
504	26	26
505	33	X^2
506	54	)
507	65	×
508	43	RCL
509	22	22
510	95	=
511	42	STO
512	25	25
513	69	OP
514	06	06
515	98	ADV
516	98	ADV
517	98	ADV
518	91	R/S
519	76	LBL
520	16	A'
521	47	CMS
522	69	OP
523	00	00
524	81	RST
525	00	0
526	00	0
527	00	0
528	00	0
529	00	0
530	00	0
531	00	0

060	11	A
081	12	B
102	13	C
124	18	C'
142	23	LNX
234	44	SUM
254	14	D
310	15	E
323	95	=
364	53	(
374	54	)
520	16	A'

Transformer test program calculates series resistance

5. Determine what maximum flux density (including peak level) the core can sustain without saturating. Enter this value (in G) and press E′.

6. Enter the inductance constant A_L (in H/N^2) and press A.

7. Enter the effective core area (in cm^2) and press B.

8. Enter effective window area (in cm^2) and press C.

9. Determine the mean turn length (in cm), enter this value and press D.

10. Select an appropriate fill-factor percentage, enter this value and press E. The winding configurations and amount of insulation used will influence this decision. For this example, assume an arbitrary 50% fill factor.

11. Press SBR and = keys. This step sets the program in motion to produce the transformer design information **(Table 3)**. If you're not using a printer, you can recall results after program execution from the data registers indicated in **Table 3.**

TABLE 3—DESIGN-PROGRAM OUTPUT

PRINTER OUTPUT		DESCRIPTION	MEMORY REGISTER
8.6—06	AL	INDUCTANCE CONSTANT (H/N^2)	R_{01}
1.38	CCM^2	EFFECTIVE CORE AREA (cm^2)	R_{02}
0.587	WCM^2	EFFECTIVE WINDOW AREA (cm^2)	R_{03}
6.2	MTRN	MEAN TURN LENGTH (cm)	R_{04}
50.	%FIL	FILL FACTOR (%)	R_{05}
100.	VIN	DC SOURCE VOLTAGE (V)	R_{06}
400.	VOUT	RMS OUTPUT VOLTAGE (V)	R_{07}
0.25	IOUT	RMS OUTPUT CURRENT (A)	R_{08}
30000.	HZ	OPERATING FREQUENCY (Hz)	R_{09}
1500.	GAUS	MAXIMUM CORE FLUX DENSITY (G)	R_{10}
SW		TRANSFORMER TYPE	
72.	NPRI	PRIMARY TURNS	R_{13}
25.	AWGP	PRIMARY WIRE SIZE (AWG)	R_{19}
161.	NSEC	SECONDARY TURNS	R_{12}
29.	AWGS	SECONDARY WIRE SIZE (AWG)	R_{16}
2.236111111	1:A	TURNS RATIO	R_{24}
344.3168815	JPRI	PRIMARY CURRENT DENSITY (A/cm^2)	R_{25}
389.307893	JSEC	SECONDARY CURRENT DENSITY (A/cm^2)	R_{23}
0.0445824	LPRI	PRIMARY INDUCTANCE (H)	R_{20}
.2360140169	CU	COPPER LOSS (W)	R_{26}
0.2476	CORE	CORE LOSS (W)	R_{27}
99.51871355	%	TRANSFORMATION EFFICIENCY	

Checking the results

No design is complete without some sort of confirmation, and the test program **(Table 2)** lets you run a preliminary bench check. Using the expressions

$$k = \sqrt{\frac{L_{OC} - L_{SC}}{L_{OC}}}$$

and

$$L' = L_{OC}(1 - k)(1 + A^2),$$

where L_{OC} and L_{SC} are the primary-winding inductances with the secondary open- and short-circuited, respectively, and A is the turns ratio, it performs the standard open-circuit- versus short-circuit-secondary winding test to determine the leakage inductance (L′) and coupling coefficient (k).

The program is set up to accommodate the two sets of data (open- and short-circuit measurements). To use it, proceed as follows:

1. Press A′ to initialize the program.

2. Enter the secondary open-circuit current, voltage and leading or lagging time delay (in sec) using A, B and C keys, respectively. If you've monitored the phase angle, enter this value (in degrees) with C′.

3. Enter secondary short-circuit current, voltage and leading or lagging time delay (in sec) using A, B and C keys, respectively. If a phase-angle value is available, enter it using C′.

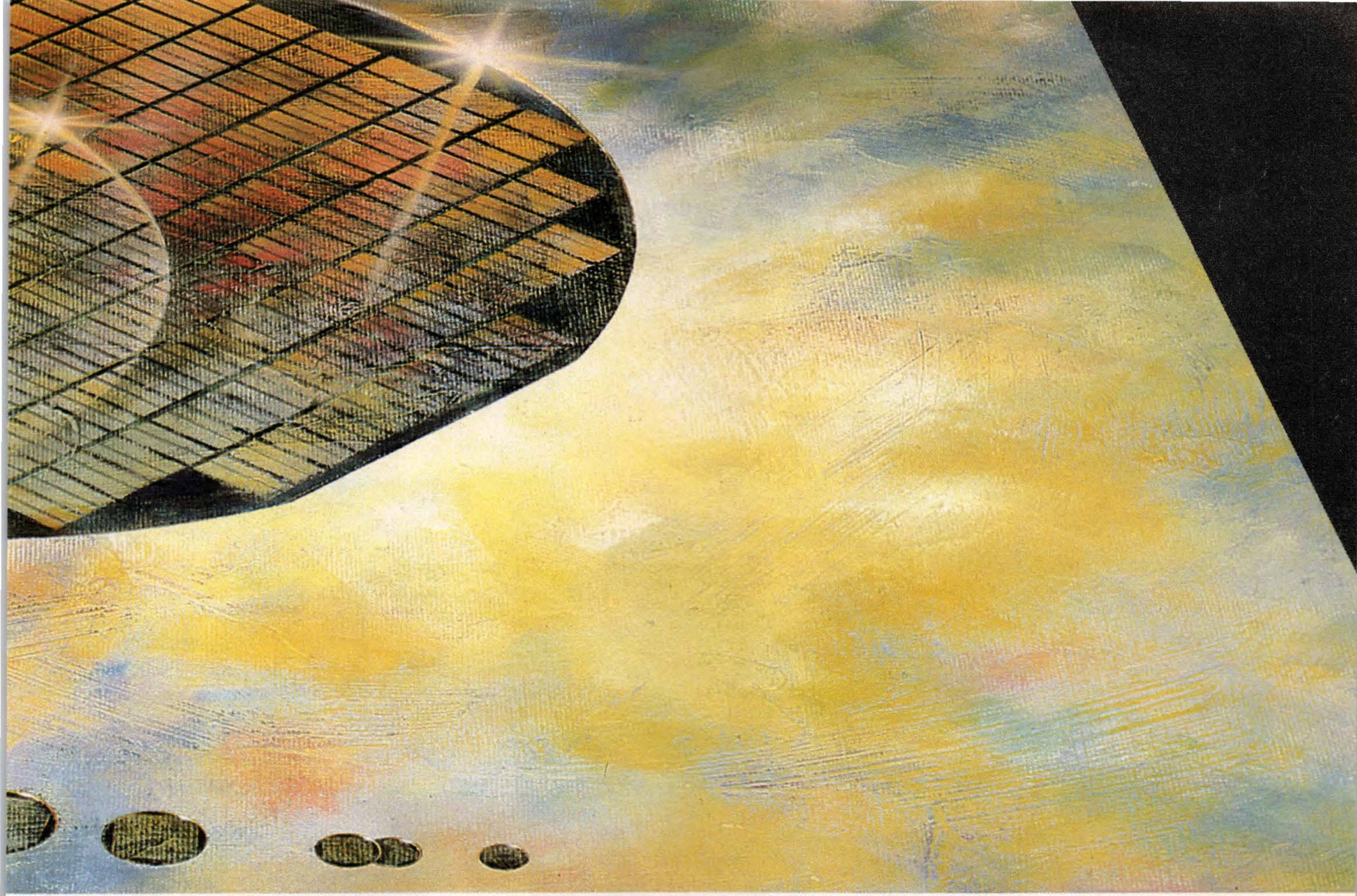
Note: Be consistent in both steps—use either the time delay between current and voltage waveforms read from an oscilloscope or the phase angle as read from a phase meter.

4. Enter operating frequency using D.

The program then calculates and prints the equivalent series impedance R+jX. (The series-resistance value represents the copper and core resistive losses.) The real and imaginary parts of the series are labeled RS and XS, respectively, on the printer output. **EDN**

Author's biography

Gerald West is a principal development engineer at Honeywell's Marine Systems Operations (Seattle, WA), where he is currently involved in the design and development of sonar electronics systems. A licensed pilot, he received his BS degree in physics from the University of Washington and has been with Honeywell for 26 yrs.



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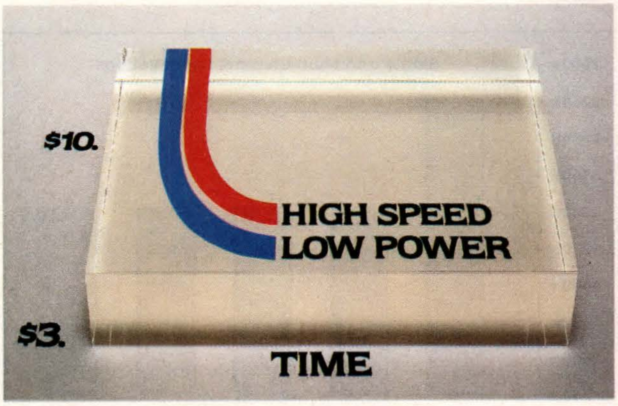

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CIRCLE NO 55

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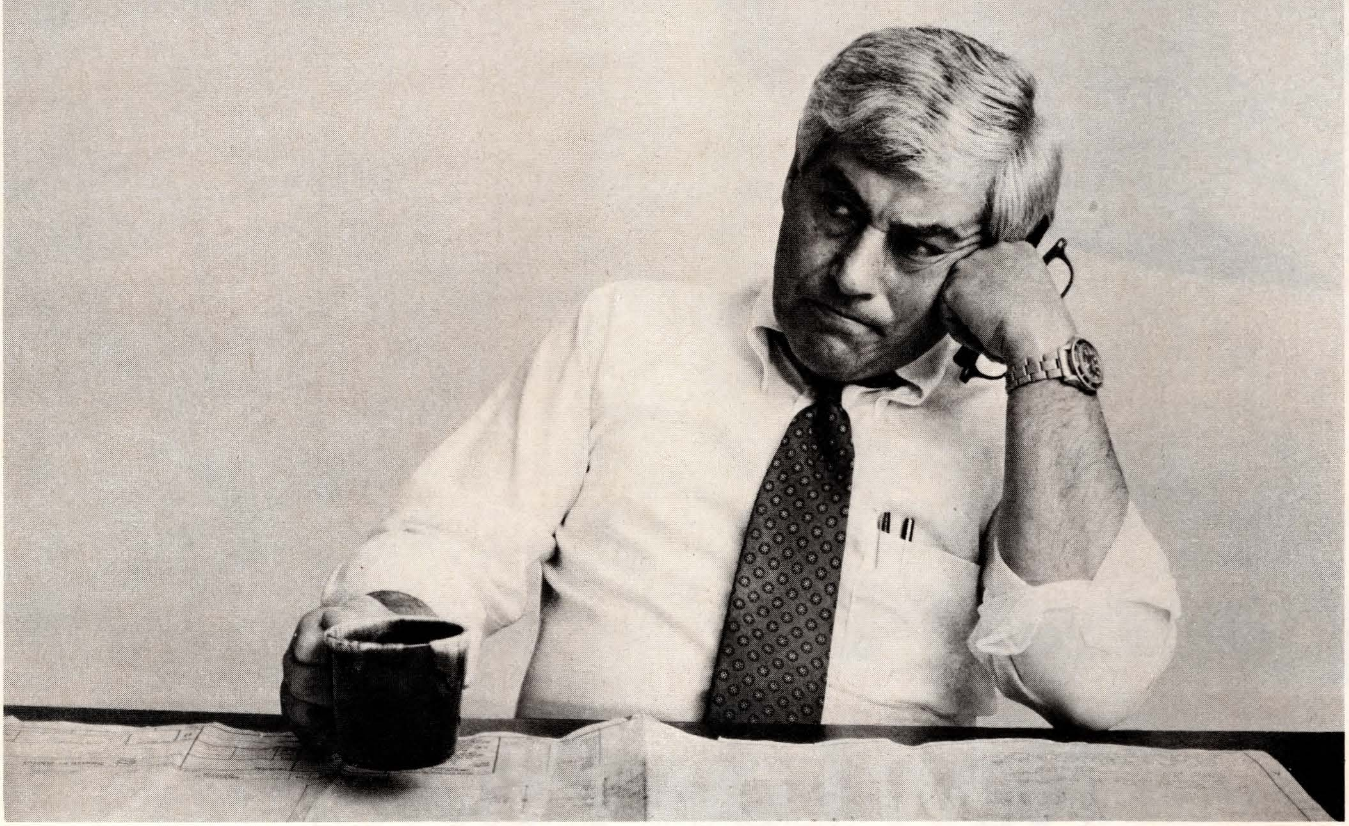

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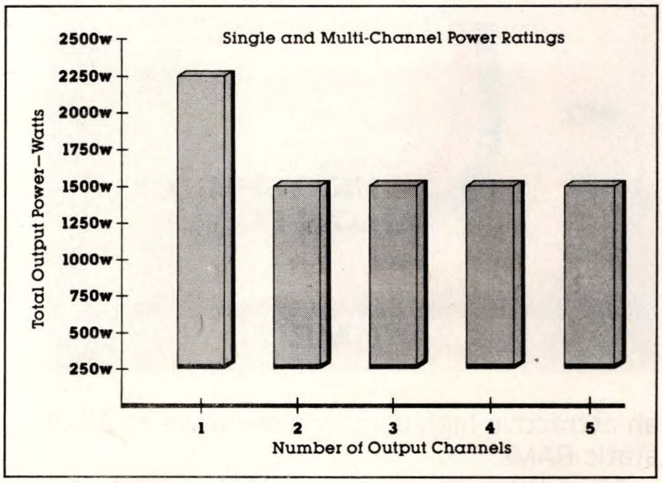

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CIRCLE NO 56

Simplify hard-disk interfaces with a VLSI controller

A new hard-disk controller IC eliminates a board full of MSI and SSI devices from µP/disk interface circuits. With its high-level command set, the chip also eases data-transfer-software development.

Henryk Szejnwald and **Phil Brooks,** NEC Electronics

You can simplify microprocessor/hard-disk interfaces by using the µPD7261 hard-disk controller (HDC) IC. Coupled with a DMA controller and a few logic chips, the HDC supports Storage Module Drive (SMD) units as well as Winchesters having floppy-like connections.

The µPD7261 consists of three major sections: a high-speed format controller, an 8-bit CPU and a µP interface. The format controller accommodates a variety of data formats at bit-transfer rates to 12 MHz; the CPU, through its multifunction I/O ports, handles the drive interface, and the µP-interface section connects to the host processor. The 40-pin IC operates from one 5V supply and offers TTL compatibility on all I/O lines except two clock pins. (For a more detailed discussion of HDC architecture, see **box,** "Inside the µPD7261.")

As an example of the HDC's interface capability, consider **Fig 1a**'s SMD interface circuit. The µPD7261 controls as many as eight drives through three unit-select outputs, and five TAG signals allow eight of the controller's programmable I/O lines to serve multiple functions. In the SMD mode, the HDC derives its write-clock signal from connected drives; two multiplexers driven by the HDC's Sync output direct data and clocks into and out of the controller chip.

The µPD7261's clock and data signals, as well as all single-function control lines (BT0, BT1, INDEX, SCT and the five TAG outputs), connect to SMD-type drives through differential line drivers and receivers. The 8-bit multifunction port communicates through a bidirectional interface that multiplexes drive-status inputs and control outputs. A LOW on the HDC's BDIR output signifies a status-input mode and selects the Fault, Seek-error, On-cylinder, Unit-ready, Am-found, Write-protected, Seek-end and Unit-selected drive lines. A HIGH BDIR level indicates a control-write operation, and an 8-bit latch stores the states of BT2 through BT9 after HIGH-to-LOW BDIR transitions.

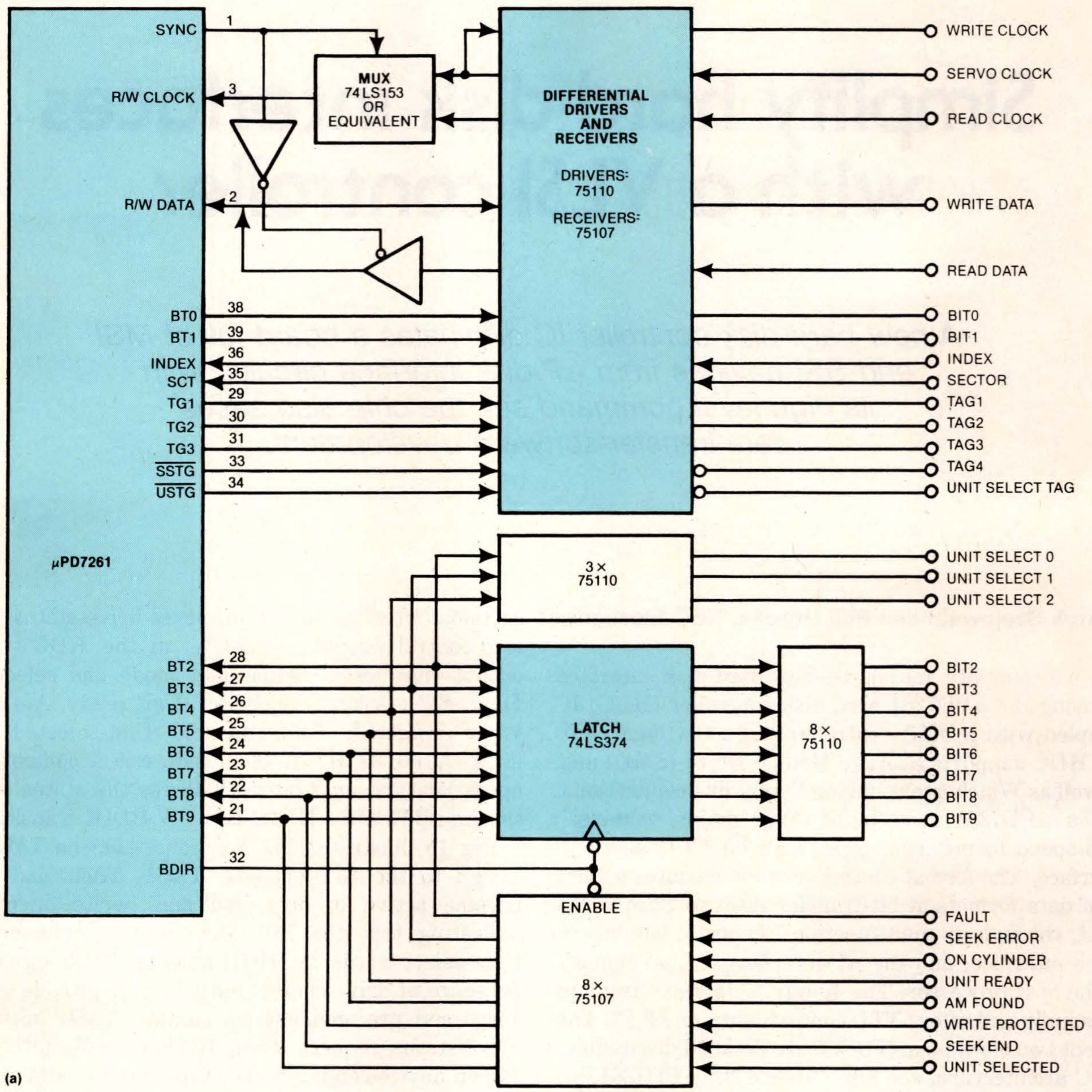
Fig 1b illustrates the functions that the TAG lines assign to the BIT outputs. TAG1, TAG2 and TAG3 become active in data-read and -write operations, indicating that the BIT lines contain cylinder- and head-select words. A HIGH level on TAG3 signals the presence of drive-control outputs that provide gating, servo and precompensation signals. TAG4 initiates a drive-status request using BIT9 to differentiate between device-condition and -type interrogations.

Floppy-like interface

A more common interface than the SMD circuit, the floppy-like-hard-disk interface (**Fig 2**) mimics the connections between floppy-disk drives and their controllers. Unlike the SMD interface's I/O lines, data and control signals in the **Fig 2** circuit perform only one function and thus allow simpler driver configurations. When switched into the floppy-like mode, the µPD7261's internal CPU reassigns its programmable I/O lines for compatibility with Seagate ST506-type interfaces (note that the chip's signal names change to reflect their new functions).

In the floppy-like configuration, only read- and

Programmable I/O lines serve multiple functions



(a)

OUTPUT	TAG1 CYLINDER SELECT	TAG2 HEAD SELECT	TAG3 CONTROL SELECT	TAG4 SENSE SELECT
BIT0	(LSB) 1	(LSB) 1	WRITE GATE	—
BIT1	2	2	READ GATE	—
BIT2	4	4	SERVO +	—
BIT3	8	—	SERVO −	—
BIT4	16	—	FAULT ERROR	—
BIT5	32	—	—	—
BIT6	64	—	RETURN TO ZERO	—
BIT7	128	—	STROBE EARLY	—
BIT8	256	—	STROBE LATE	—
BIT9	(MSB) 512	—	—	DEVICE TYPE REQUEST

(b)

Fig 1—An SMD interface (a) *requires a data latch and an array of differential line drivers and receivers. The μPD7261's programmable I/O lines allow eight interface signals (BT2 through BT9) to handle 19 input and output functions. Four TAG signals determine the roles of the BIT signals* **(b).**

write-data connections require differential transmitters and receivers; all other lines can employ simple TTL buffers. To reduce system size and cost, the controller's internal processor assigns output senses to the I/O control lines, minimizing the number of IC packages the interface requires. The circuit uses six 7406 inverters (one fully utilized package), five 7407 buffers (one package with one spare buffer) and six 74LS14 Schmitt-trigger inverters (one package). In addition, the interface requires a 2- to 4-line decoder (a 74LS139 or equivalent) to convert the HDC's 2-line unit-select code to four discrete device-select outputs.

To complete this interface, you must add a phase-locked loop to derive a read clock from the modified frequency-modulated disk data. Furthermore, you must furnish a precompensation circuit that converts the HDC's early and late precompensation signals to write delays.

The PLL circuit **(Fig 3)** employs a phase comparator and loop filter optimized for clock-recovery applications. The loop locks to incoming data streams by setting the VCO to a frequency that centers clock transitions within a 50-nsec pulse generated by input one-shot IC_4. IC_1 and IC_3 provide VCO control signals by matching IC_4's Q output against the oscillator's complementary C and $\overline{C}$ lines. When the loop is locked, both NAND-gate outputs go LOW for equal intervals; an unlocked condition causes unequal output pulses. To maintain a locked loop, a LOW level at IC_1's output must increase the VCO's frequency, and LOW signals at IC_3's output must decrease the clock rate.

To allow the increase- and decrease-frequency voltages to share one control line, IC_2 inverts IC_1's output, and diodes D_1 and D_2 isolate the phase comparator from the loop filter. D_1 and IC_2 source current into the filter circuit when the VCO's frequency must increase; D_2 and IC_3 draw current out of the filter network to decrease the clock rate. While the loop remains locked, equal-duration increase-frequency and decrease-frequency ramps cause the integrated filter output to maintain a constant level **(Fig 3b)**. An unlocked condition **(Fig 3c)** results in unequal control ramps and thus generates a frequency-correction level.

Free-run control R_1 minimizes the PLL's lock-up time by establishing a quiescent VCO frequency close to the disk's nominal 10-MHz read rate. If your circuit's VCO drifts in the absence of read data, you can maintain minimum lock times by using a multiplexer to feed the crystal-stabilized write clock into the read-data input during data-free intervals. With such a reference signal, the VCO remains stable regardless of component drift.

In addition, you can minimize clock jitter and bit-error rates by carefully selecting one-shot and loop-filter components. **Fig 3a**'s filter values represent typical components for use with ST506-type drives, but actual values depend largely on specific drives and data rates. Likewise, IC_4's 50-nsec output-pulse duration results in an optimum compromise between VCO tracking and lock-up speed for typical drives; you might need to experiment with timing values in your application. Be certain, though, to use a silver-mica or equally

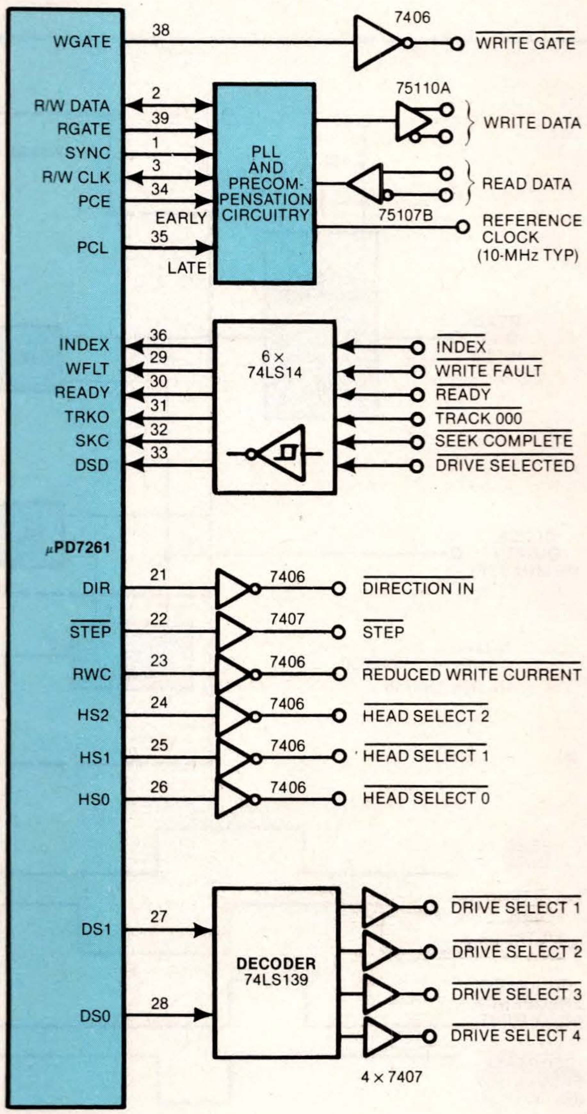


Fig 2—Simplifying floppy-interface-like connections, *the HDC's control-line polarities minimize the required number of external IC packages. Unlike* **Fig 1**'s *SMD interface, this circuit requires differential drivers and receivers only on data lines. However, it does require an outboard PLL and a precompensation network* **(Figs 3 and 4).**

Floppy-like connection minimizes external logic

stable capacitor in the one-shot's timing circuit; units with less stable dielectrics introduce clock-rate errors.

Anticipate errors

To compensate for predictable bit-position errors arising from disk magnetic properties, random noise or flux-change delays in read/write heads, the μPD7261 provides early and late precompensation signals. The controller monitors write-data streams, recognizing bit patterns that require timing changes for improved data recoverability. SMD-type drives handle such precom-

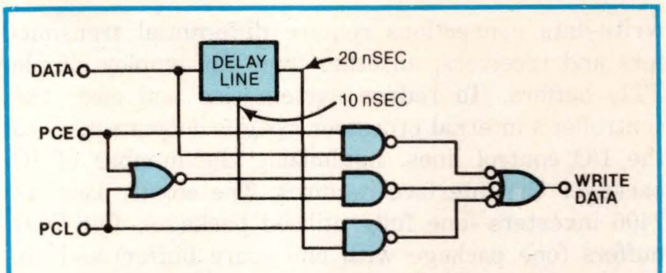


Fig 4—A precompensation circuit *uses early and late correction signals to properly delay write data. An early signal eliminates 10 nsec of propagation time from the write-data path; a late command adds a 10-nsec write delay.*

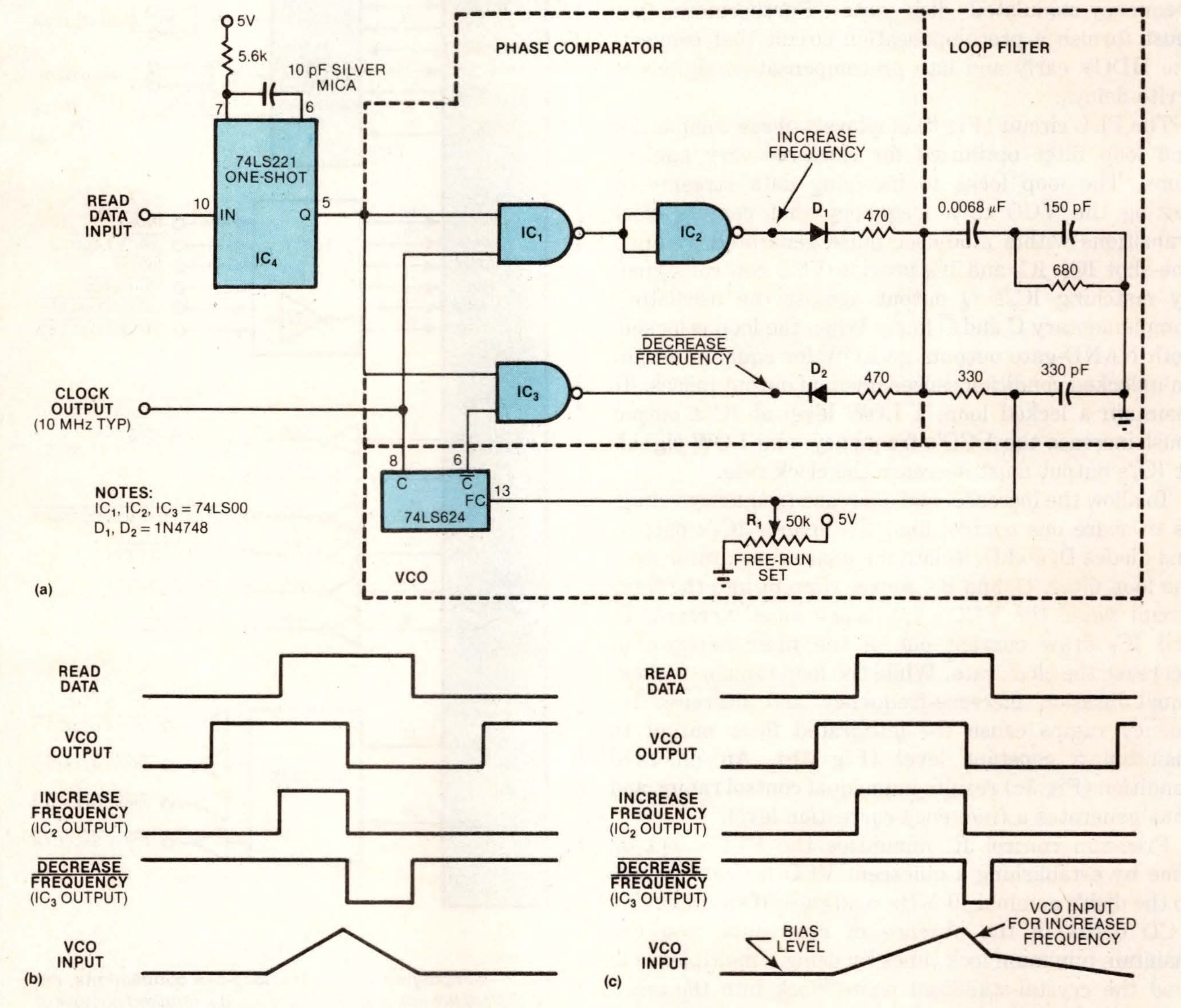
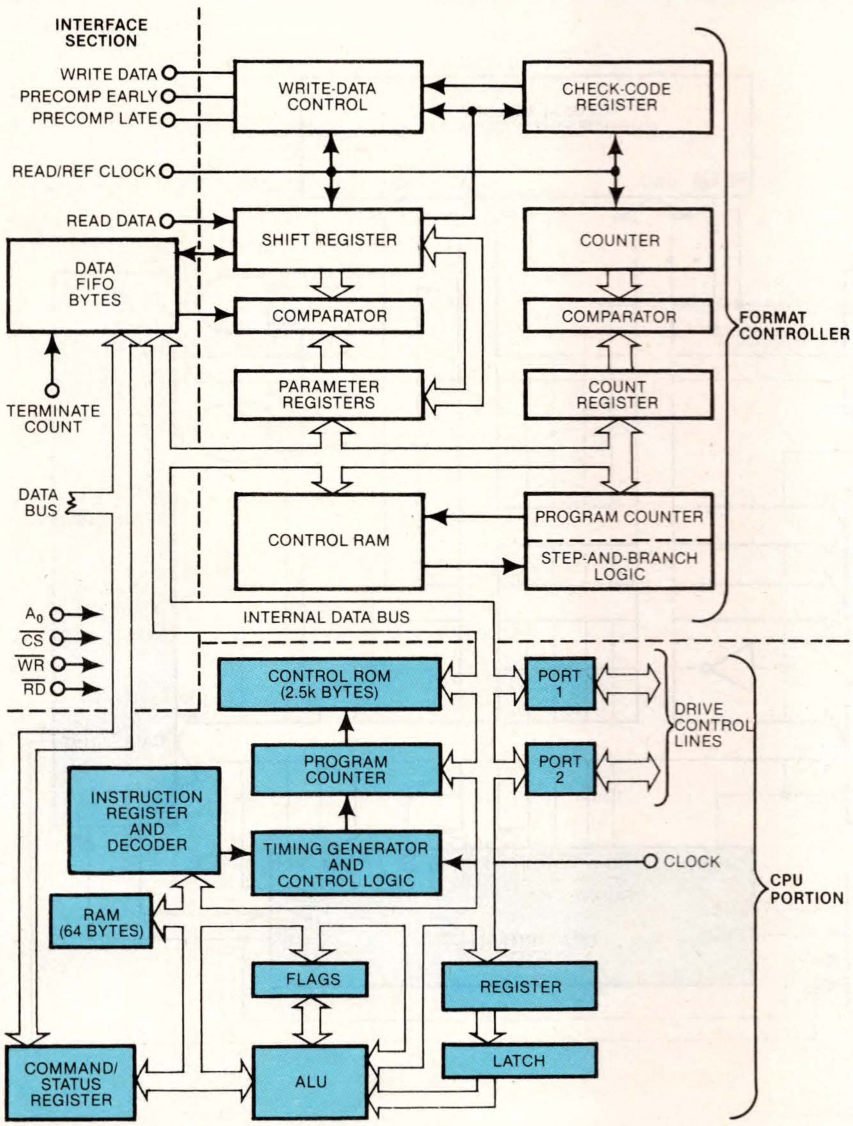


Fig 3—By quickly locking to read-data bursts, *a PLL* **(a)** *generates stable clock signals for the* **Fig 2** *interface. Increase- and decrease-frequency control signals servo the VCO's frequency to maintain clock transitions at the center of IC_4's 50-nsec output pulse. During locked conditions* **(b)**, *IC_2 sources control current through D_1 for 25 nsec, IC_3 draws current through D_2 for 25 nsec and the VCO's control voltage remains constant. Unlocked conditions* **(c)** *cause unequal control-voltage ramps and result in corrected clock rates.*

Inside the μPD7261

The μPD7261 derives its functions from three major chip sections: an 8-bit CPU similar to several widely used single-chip μCs, a format controller that includes a 32-word, 16-bit writable-control-store register, and a μP interface **(figure).** By performing all major data formatting and drive-control functions internally, the device eliminates most of the circuitry typical of hard-disk/μP interfaces and provides a high-level, optimized command set that simplifies software design. (See **box,** "Speaking the hard-disk language.")



An internal CPU *provides the μPD7261's control and interface functions. A high-speed format controller handles all data operations, and the HDC's interface circuit includes an 8-bit FIFO to buffer data and command strings.*

The μPD7261's internal μP furnishes the controller's configurable drive interface through 16 programmable I/O lines. The line's functions and data directions depend on the controller's operating mode, and by optimizing each line's role, the CPU minimizes external-logic requirements. In addition to providing programmable I/O, the controller's CPU includes 2.5k bytes of ROM and 64 bytes of RAM.

The second major chip section, the format controller handles all read, write and error-correction functions. Based on a serial-to-parallel-to-serial converter, it identifies address marks and compares disk data streams with user-defined search bytes. The controller also performs all data-verification and format-specification functions. When executing commands, it derives its control data from the CPU's ROM, and a high-speed sequencer manages controller activity at the disk's data-transfer rate.

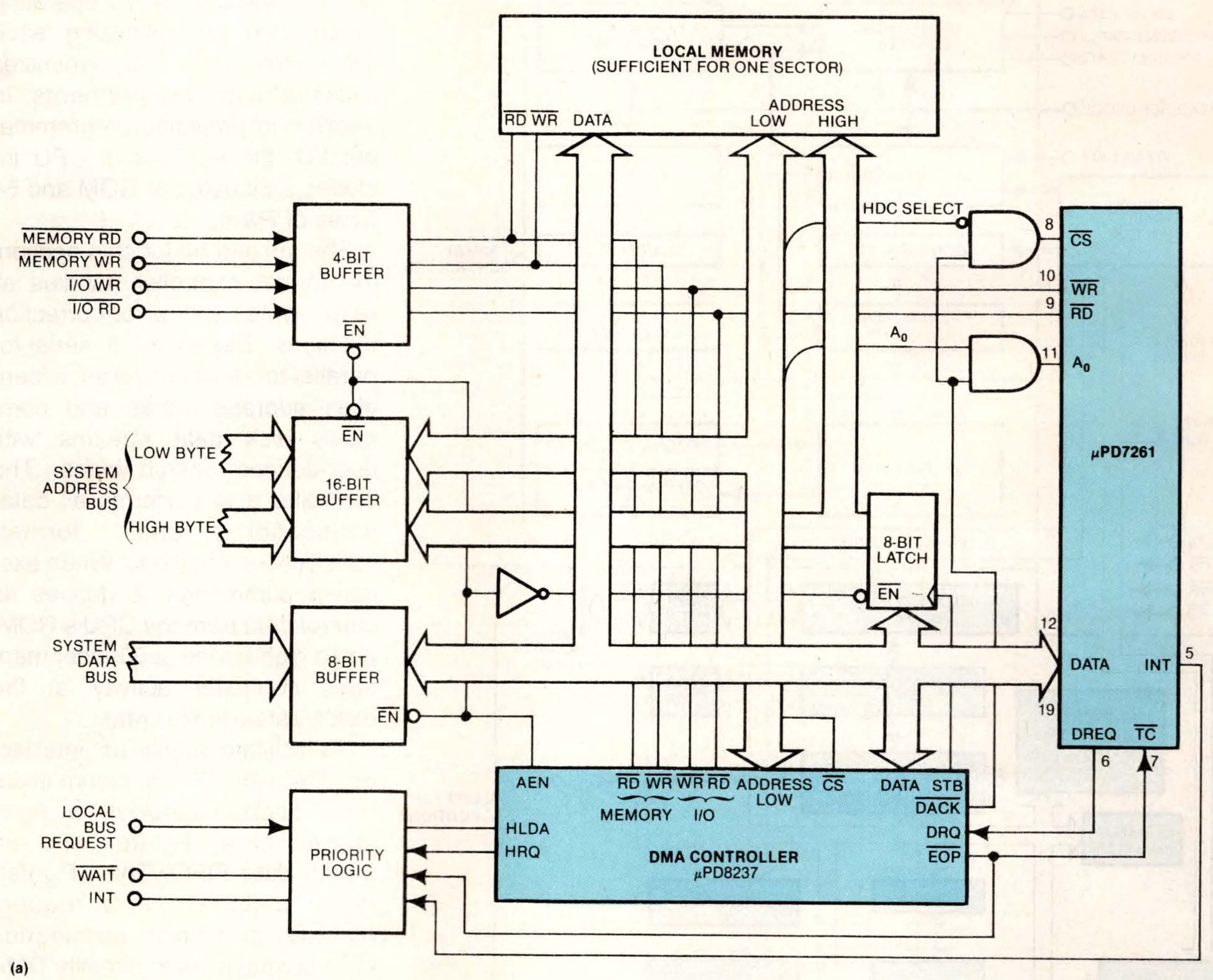
To facilitate simple μP interfaces, the μPD7261's communications section employs a command/status register and an 8-byte data FIFO. The μP interface includes data-request (DREQ) and count-termination ($\overline{TC}$) control lines to simplify DMA connections; the data FIFO reduces parameter-entry cycle times by allowing a host μP to enter multibyte command specifications at transfer rates to 1M bytes/sec.

For more information on the μPD7261, **Circle No 743.**

pensation internally; floppy-like drives require external delays.

Fig 4 illustrates a precompensation circuit that provides ±10-nsec timing variations. A tapped delay line provides outputs with 10- and 20-nsec data delays; normal operations employ data from the 10-nsec tap, and early and late cycles use the input and 20-nsec signals, respectively. ±10-nsec compensation satisfies most ST506-type applications, but check your drive's data sheet to determine the optimum delays for your system.

After designing your system's HDC/drive interface, carefully consider the controller's μP connections. Because of the μPD7261's high read/write data rates, you'll probably need a block of local memory and a DMA controller to provide a buffer between the HDC and your system's μP bus. Hard-disk drives often transfer data at bit rates to 12 MHz, so the controller/memory interface must be capable of handling byte-transfer cycles as short as 660 nsec. Although more expensive and more complicated than direct bus connections, DMA interfaces allow such high-speed read and write



CS	A_0	RD	WR	REGISTER
0	0	0	1	READ } DATA
0	0	1	0	WRITE } REGISTER
0	1	0	1	COMMAND REGISTER
0	1	1	0	STATUS REGISTER
0	X	1	1	} DON'T CARE
1	X	X	X	
0	X	0	0	HDC INHIBITED

(b)

Fig 5—Employing a DMA controller *and a block of local memory, the μPD7261's μP interface* **(a)** *allows fast data transfers. You can program 2-stage read and write operations by instructing the DMA controller to move data into and out of system memory before and after disk operations. Thus, the local memory stores data only during active HDC cycles. The register organization* **(b)** *simplifies command transfers.*

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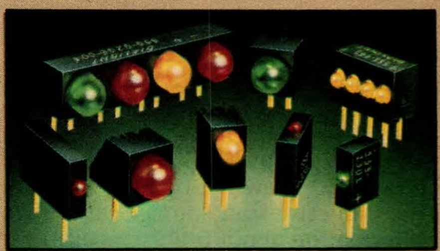

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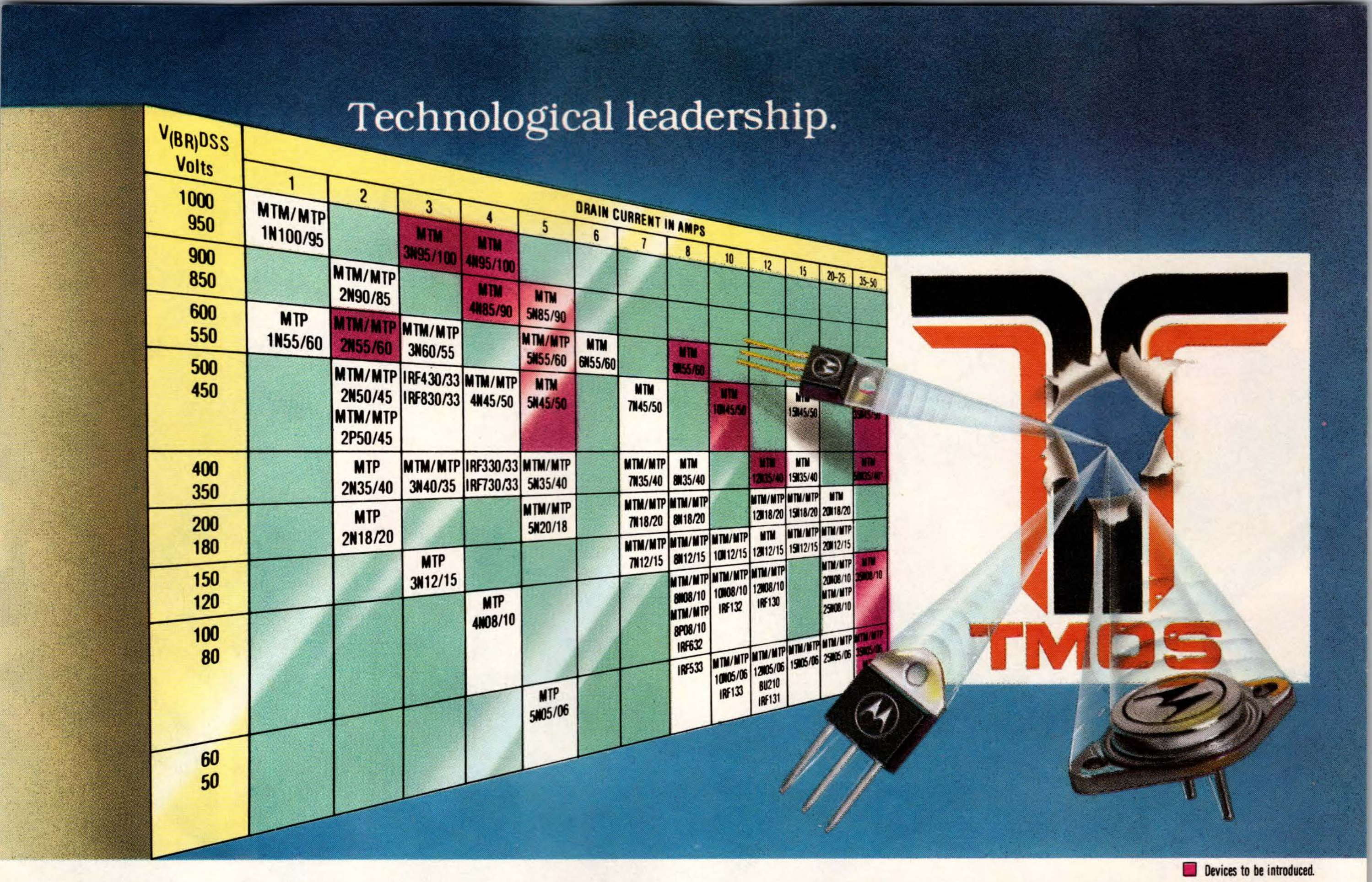

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City ____________ State ________ ZIP ________ operations and become especially attractive in applications requiring fast transfers of large data blocks.

A typical system interface (**Fig 5**) employs a μPD8237 DMA controller and a local memory array large enough to hold the largest data block you expect to transfer in one operation (usually one disk sector). To optimize data throughput, you can use the DMA controller's multiple-transfer-mode capability to perform read and write operations in two steps.

For example, to initiate a sector-read operation using **Fig** 5's interface scheme, first program the DMA controller for a memory-to-memory transfer by storing a source address (a location within the local memory) in the chip's channel 0 register and a destination address (within the main system memory) in channel 1. Then instruct the controller's channel 2 logic to effect an HDC-to-memory transfer of one sector's data. A Read Sector command fed to the HDC initiates the disk-read operation, with the DMA controller storing successive data bytes in local memory.

After the HDC has taken one sector's data from the disk, an interrupt output signals the host μP to request

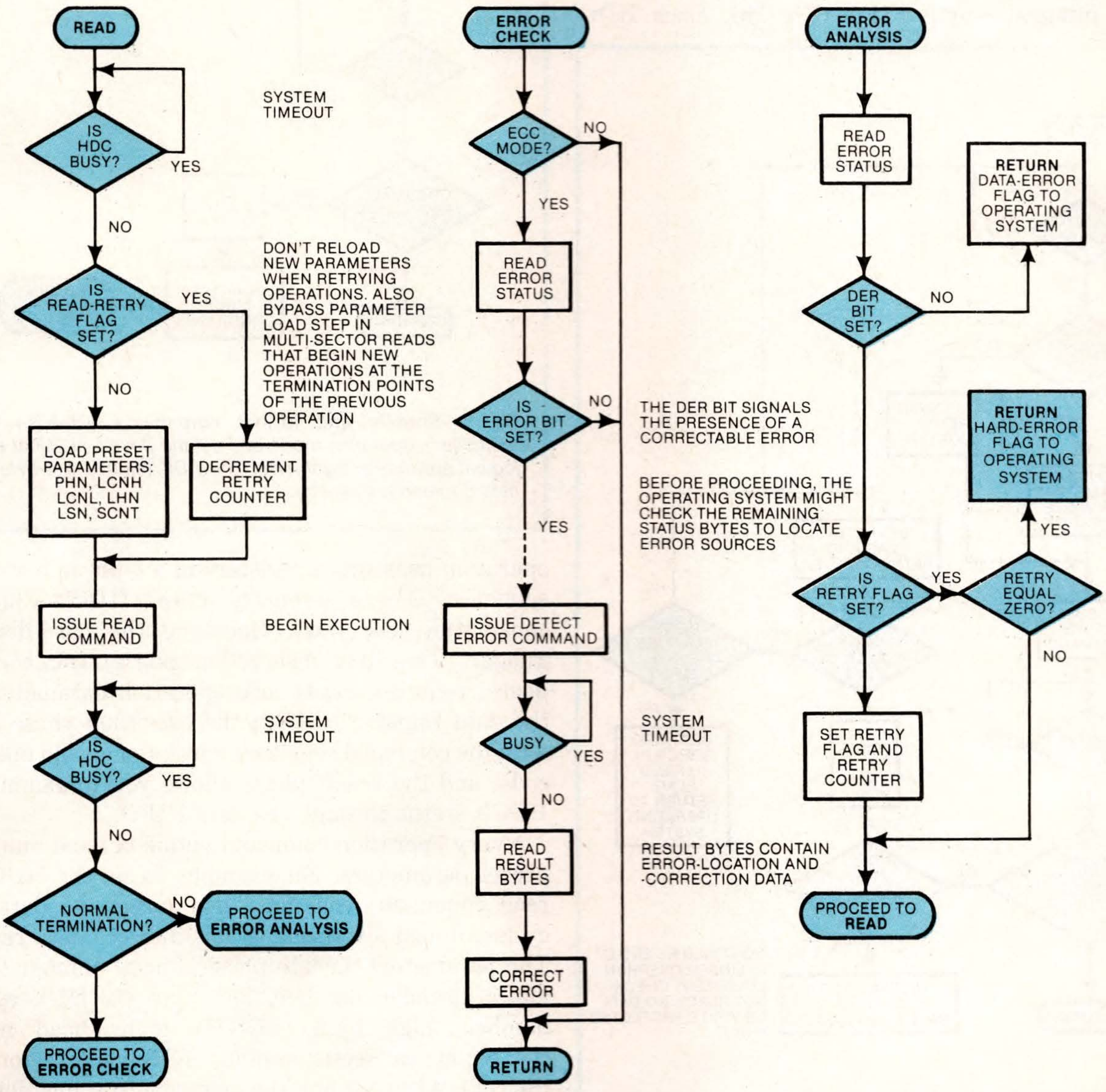

Fig 6—A typical data-read cycle *includes command, execution and result phases. After an instruction-cycle termination, the host μP must interrogate the HDC's status register to confirm error-free command execution.*

a memory-to-memory data transfer through the DMA controller. An $\overline{EOP}$ output from the μPD8237 signals a completed transfer and indicates that disk data resides in the main system memory. You can program write operations by reversing the process: First move data from the main memory to the local array and then invoke a memory-to-I/O transfer. Alternatively, you can eliminate the DMA controller by employing high-speed dual-ported system memory or by designing a large FIFO buffer into the HDC/system interface.

Parameter stack eases command entry

To simplify programming, the HDC includes command and status registers as well as a data register with an integral 8-byte FIFO **(Fig 5b).** Each HDC operation uses these registers in a 3-phase instruction sequence. (For a summary of the HDC's Command capabilities, see **box,** "Speaking the hard-disk language." The first instruction phase, the command phase, requires you to load operation parameters into the data register's FIFO; the execution phase begins with the command register's receipt of a valid operation code, and the result phase allows you to examine the HDC's status through the data FIFO.

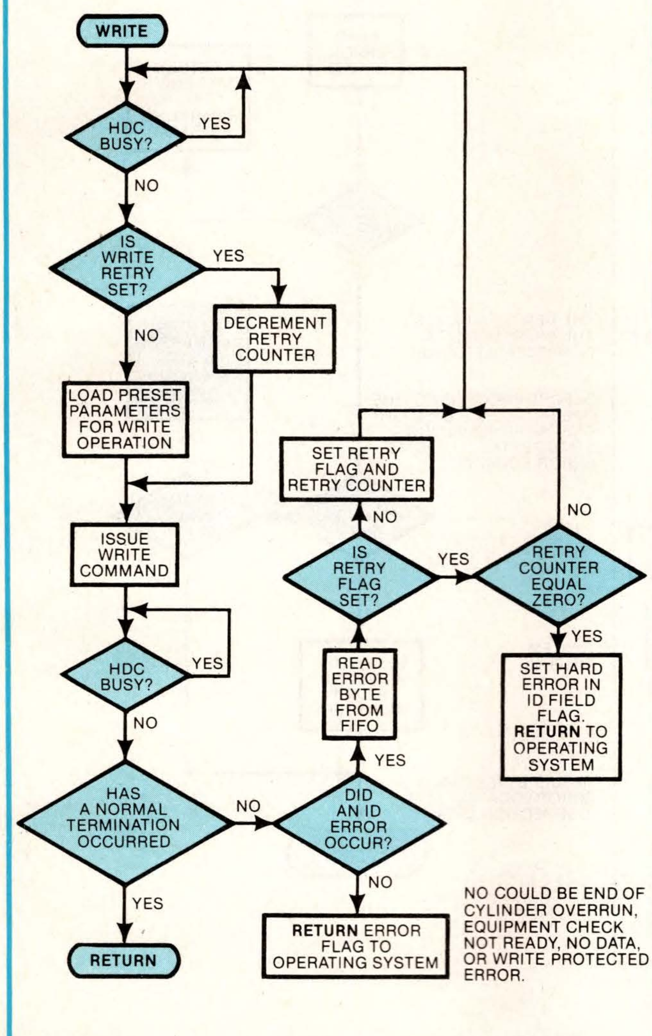

Fig 7—Writing data to a disk *involves a program flow similar to* ***Fig 6****'s read routine. The program returns error flags to the μP's operating system if drive conditions prevent a successful write operation.*

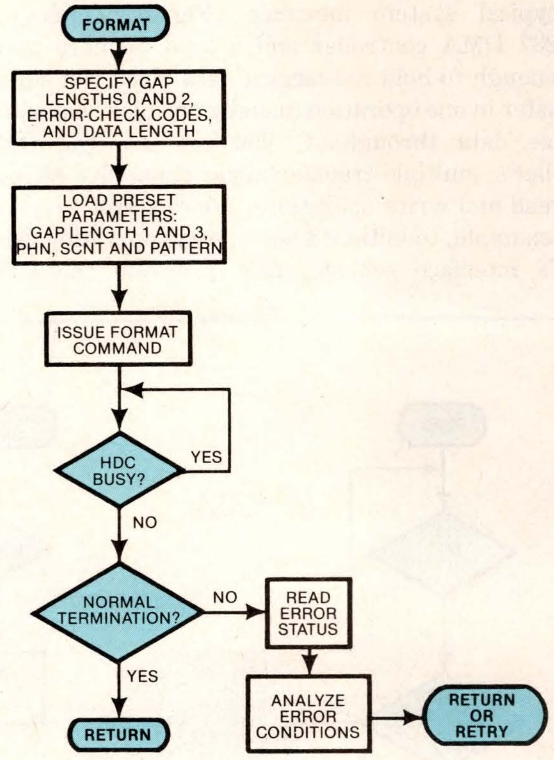

Fig 8—Specify and format commands *establish the controller's operating mode and set the drive's physical and logical address assignments. The HDC records a 4-byte ID field on each disk sector.*

Every operation command entails a fixed number of preset parameters. For example, to set the HDC for a read command, you must use successive data-write cycles to load six specifications into the data register. The parameters include physical-head number (PHN); logical-cylinder number, low byte (LCNL); cylinder number, high byte (LCNH); logical-head number (LHN); logical-sector number (LSN); and sector count (SCNT). After loading the operation specifications, the host μP initiates the execution phase by writing a data-read instruction to the command register.

When the HDC has completed its execution cycle, it signals the host μP with an interrupt. The μP then

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CIRCLE NO 58

examines the status register to determine whether the operation has terminated successfully. In the event of an error, the μP can check specific results by reading successive data-FIFO bytes. The first result byte after a read operation contains error-status (EST) information that indicates the error source. The remaining FIFO bytes contain updated versions of the parameters entered during the instruction's command phase.

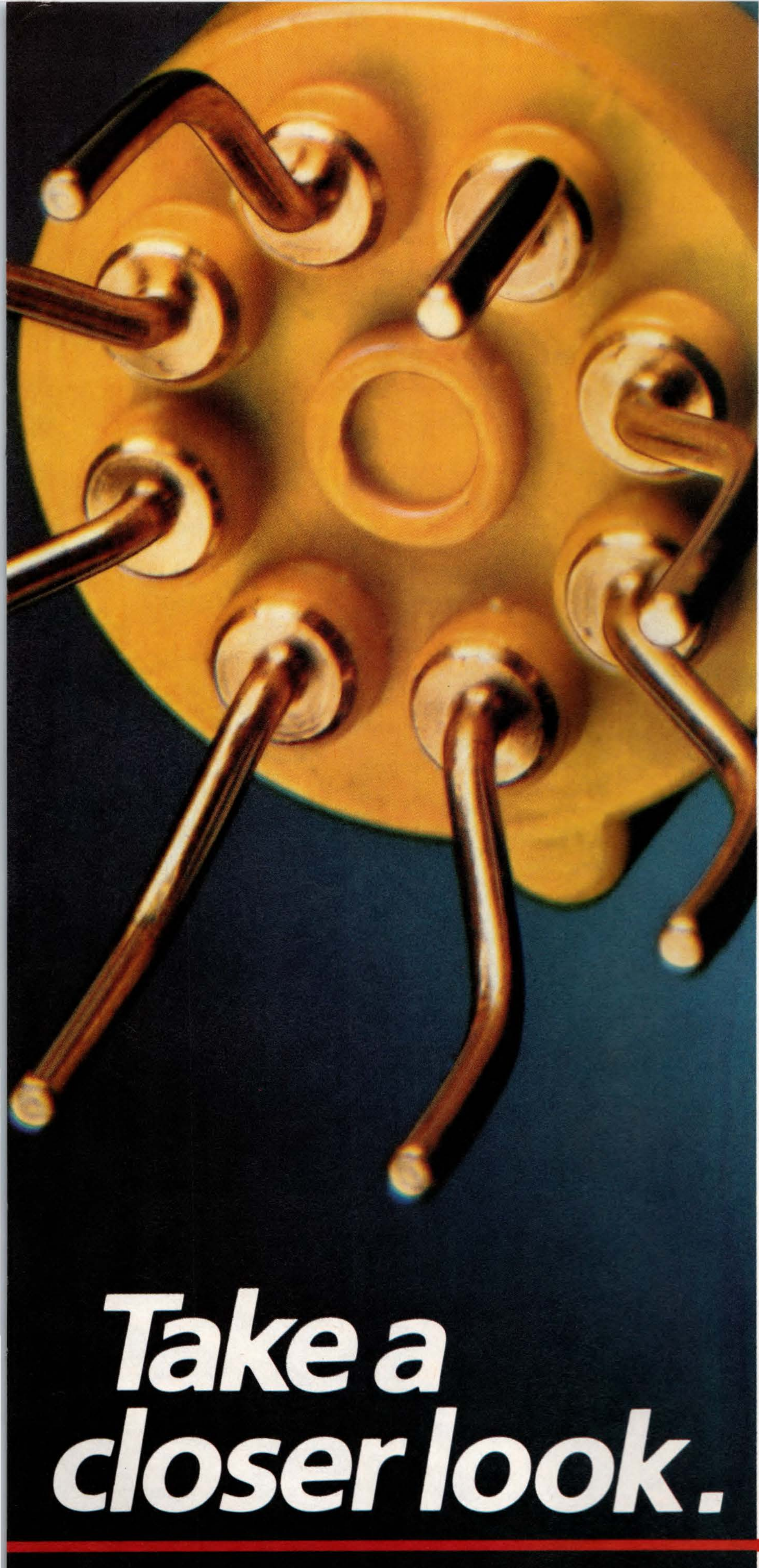
A typical data-read cycle **(Fig 6)** involves the initiation of a read command and then the complete analysis of drive and controller status. After a normal cycle termination, for instance, a system that exploits the HDC's error-correction capability must read the EST byte to check for bit errors. If the controller signals that an error exists, the μP can read the remaining result bytes to further isolate error sources, or it can directly invoke an error-correction operation. Approximately 100 μsec after the beginning of an error-correction cycle, the HDC returns five bytes that contain error-location and -pattern data. The host μP can then correct the results with an exclusive-OR operation between each faulty data byte and its corresponding correction code.

After an invalid instruction termination, the μP can

Speaking the hard-disk language

To ease software-development tasks, the μPD7261 incorporates a comprehensive command set. Each high-level instruction entails a fixed number of parametric variables that must reside in the data FIFO before command execution; the controller transfers these specifications to internal CPU registers upon beginning instruction cycles. The accompanying **table** summarizes the controller's command set and illustrates the μPD7261's ability to process complex instructions in single execution cycles.

COMMAND	DESCRIPTION
READ DIAGNOSTIC	USED ON HARD DISKS ONLY, THIS COMMAND ALLOWS THE PROGRAMMER TO READ A SECTOR OF DATA EVEN IF THE ID PORTION OF THE SECTOR IS DEFECTIVE.
READ DATA	TRANSFERS DISK DATA TO MEMORY. THE HDC CAN READ MULTIPLE SECTORS AND MULTIPLE TRACKS WITH ONE INSTRUCTION.
CHECK	DETERMINES WHETHER THE DATA PREVIOUSLY WRITTEN TO THE DISK PASSES THE CRC OR ECC POLYNOMIAL CHECK. NO DMA OPERATIONS ARE PERFORMED.
SCAN	COMPARES DATA FROM MEMORY WITH THE DATA IN A GIVEN SECTOR. IF NO MATCH OCCURS, THE HDC READS THE NEXT SECTOR AND PERFORMS THE SAME COMPARISON. THE HDC CONTINUES UNTIL THE SPECIFIED NUMBER OF SECTORS HAVE BEEN CHECKED. THE COMMAND IS TERMINATED WHEN A SECTOR WITH MATCHING DATA IS FOUND OR WHEN ALL SPECIFIED SECTORS HAVE BEEN CHECKED.
VERIFY DATA	MAKES A SECTOR-BY-SECTOR COMPARISON OF DATA STORED IN SYSTEM MEMORY BY DMA TRANSFER. AS IN READ OPERATIONS, MULTIPLE SECTORS AND TRACKS CAN BE VERIFIED WITH THIS COMMAND.
WRITE DATA	WRITES DATA FROM THE SYSTEM MEMORY, TRANSFERRED BY DMA, TO THE SPECIFIED DISK UNIT. AS IN THE READ COMMAND, DATA CAN BE WRITTEN ONTO SUCCESSIVE SECTORS AND TRACKS.
AUXILIARY COMMAND	ALLOWS EXECUTION OF FOUR ADDITIONAL FUNCTIONS: SOFTWARE RESET, CLEAR DATA BUFFER, MASK INTERRUPT-REQUEST BIT (MASKS INTERRUPTS CAUSED BY CHANGE OF STATUS OF DRIVES) AND RESET INTERRUPT CAUSED BY COMMAND TERMINATION.
SPECIFY	ALLOWS USER TO SELECT SMD OR FLOPPY-LIKE-MODE, DATA BLOCK LENGTH, ENDING TRACK NUMBER, END SECTOR NUMBER, GAP LENGTH AND TRACK AT WHICH WRITE CURRENT IS REDUCED.
SENSE INTERRUPT STATUS	WHEN A CHANGE OF DISK STATUS OCCURS, THE HDC INTERRUPTS THE HOST CPU. THIS COMMAND REVEALS THE CAUSE OF INTERRUPT, SUCH AS SEEK END, DISK READY CHANGE, SEEK ERROR, OR EQUIPMENT CHECK. THE DISK UNIT ADDRESS IS ALSO SUPPLIED.
SENSE UNIT STATUS	THE HOST CPU SPECIFIES DRIVE NUMBERS, AND THE HDC RETURNS INFORMATION SUCH AS WRITE FAULT, READY, TRACK 000, SEEK COMPLETE AND DRIVE SELECTED, OR, FOR SMD UNITS, FAULT, SEEK ERROR, ON CYLINDER, UNIT READY, AM FOUND, WRITE PROTECTED, SEEK END AND UNIT SELECTED.
DETECT ERROR	USED AFTER A READ OPERATION WHERE ECC HAS BEEN EMPLOYED. THE DETECT ERROR COMMAND SUPPLIES THE INFORMATION NEEDED TO ALLOW THE HOST CPU TO EXECUTE AN ERROR-CORRECTION ROUTINE. (ONLY ALLOWED WHEN AN ACTUAL CORRECTABLE ERROR IS DETECTED BY THE HDC)
RECALIBRATE	RETURNS THE DISK DRIVE HEADS TO THE HOME POSITION OR TRACK 000. THERE ARE THREE RECALIBRATION MODES: SMD, NORMAL OR BUFFERED.
SEEK	MOVES THE DISK-DRIVE HEADS TO THE SPECIFIED CYLINDER. AS IN RECALIBRATE, SEEK HAS THREE MODES OF OPERATION.
WRITE ID	ALSO CALLED FORMAT WRITE, THIS COMMAND IS USED TO INITIALIZE THE MEDIUM WITH THE DESIRED FORMAT, INCLUDING VARIOUS GAP LENGTHS, DATA PATTERNS AND CRC CODES. THIS COMMAND IS USED IN CONJUNCTION WITH THE SPECIFY COMMAND.
VERIFY ID	USED TO VERIFY THE ID BYTES WITH DATA FROM MEMORY. PERFORMS THE OPERATION OVER A SPECIFIED NUMBER OF SECTORS.
READ ID	USED TO VERIFY THE HEADER PORTION OF EACH SECTOR AND CHECK THE CRC FOR AN ERROR AT END OF EACH SECTOR.



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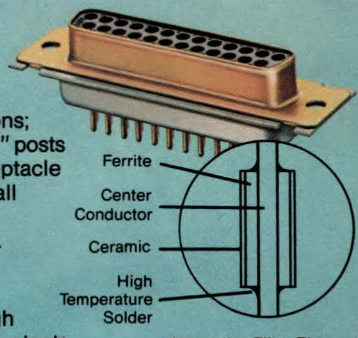

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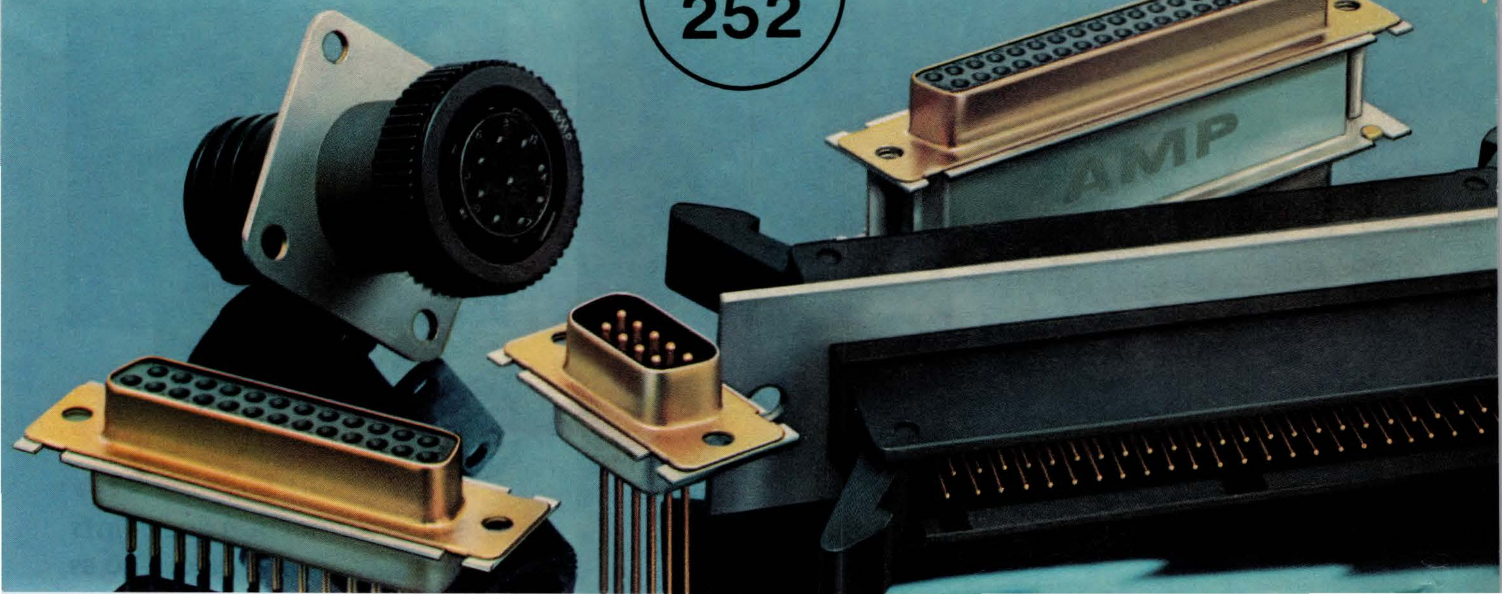


Format one track or an entire cylinder

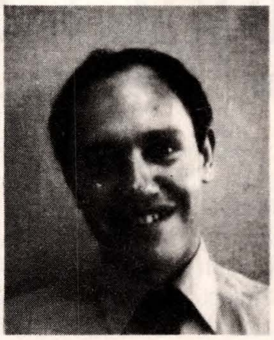
identify execution-error sources by examining the error-status byte for drive-related malfunctions. If no data error exists, the μP can attempt a retry by returning to the command's beginning after setting a retry flag. After several unsuccessful retries, the command-processing program should return program control and an error flag to the operating system. HDC write operations entail a similar program flow **(Fig 7).**

Formatting flexibility

To enter specific formats into the disk system **(Fig 8),** first invoke a specify operation. The specify command allows you to select SMD (hard-sectored) or floppy-like (soft-sectored) operation, two of the four gap lengths, CRC or polynomial error detection and block length. Next, you can begin a format cycle by loading PHN, SCNT, the data pattern and the remaining gap lengths into the data FIFO. A format command then begins the execution phase.

By independently assigning formatting parameters, you can format either one track or an entire cylinder. The format operation transfers four bytes to the disk for each assigned sector; this data includes LCNL, LCNH, LHN and LSN. The logical address data is user definable and reaches the HDC via the DMA controller and the local memory. **EDN**

Authors' biographies



Henryk Szejnwald is applications manager for computers and peripherals at NEC Electronics's Microcomputer Div (Natick, MA). Before joining NEC 3 yrs ago, he worked for Digital Equipment Corp. Henryk holds an MBA degree from Northwestern University and an MSEE from Washington University and lists reading and foreign travel as his leisure-time activities.

Phil Brooks, a product specialist at NEC's Microcomputer Div, has attended Northeastern University and served previously as manager and chief engineer at Keltron Corp. In his present position, he provides technical support for NEC's peripheral-controller products and enjoys sailing and jogging.

Article Interest Quotient (Circle One)
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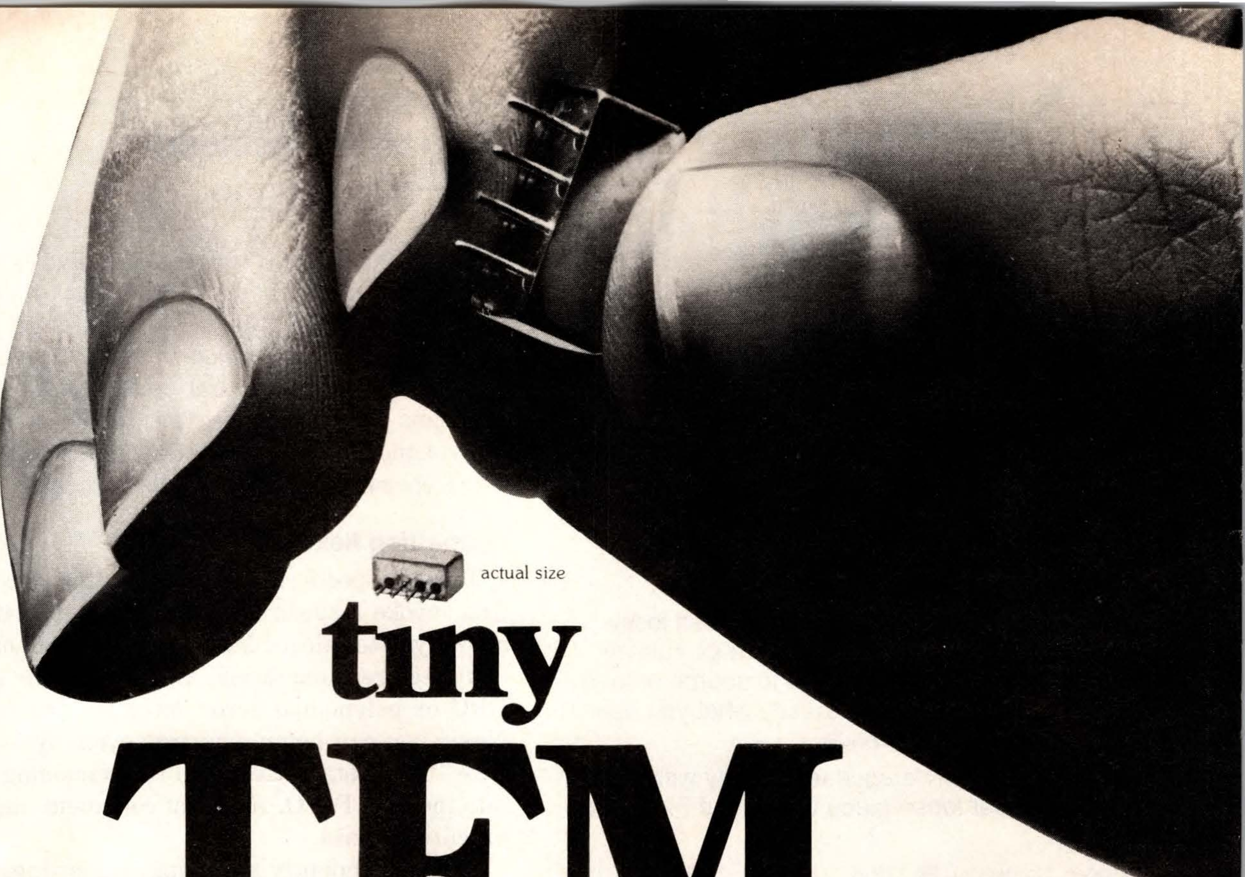

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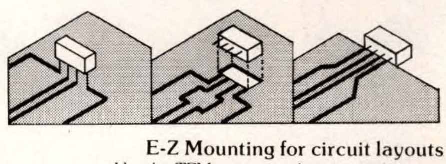

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TFM-3	.04-400	DC-400	5.3	6.0	60	55	50	45	35	35	19.95	(5-49)
TFM-4	5-1250	DC-1250	6.0	7.5	50	45	40	35	30	25	21.95	(5-49)
•••TFM-11	1-2000	5-600	7.0	7.5	50	45	35	27	25	25	39.95	(1-24)
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▪▪TFM-15	10-3000	10-800	6.3	6.5	35	30	35	30	35	30	49.95	(1-9)
▪▪TFM-150	10-2000	DC-1000	6.0	6.5	32	33	35	30	35	30	39.95	(1-9)

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CIRCLE NO 60

68 REV. A

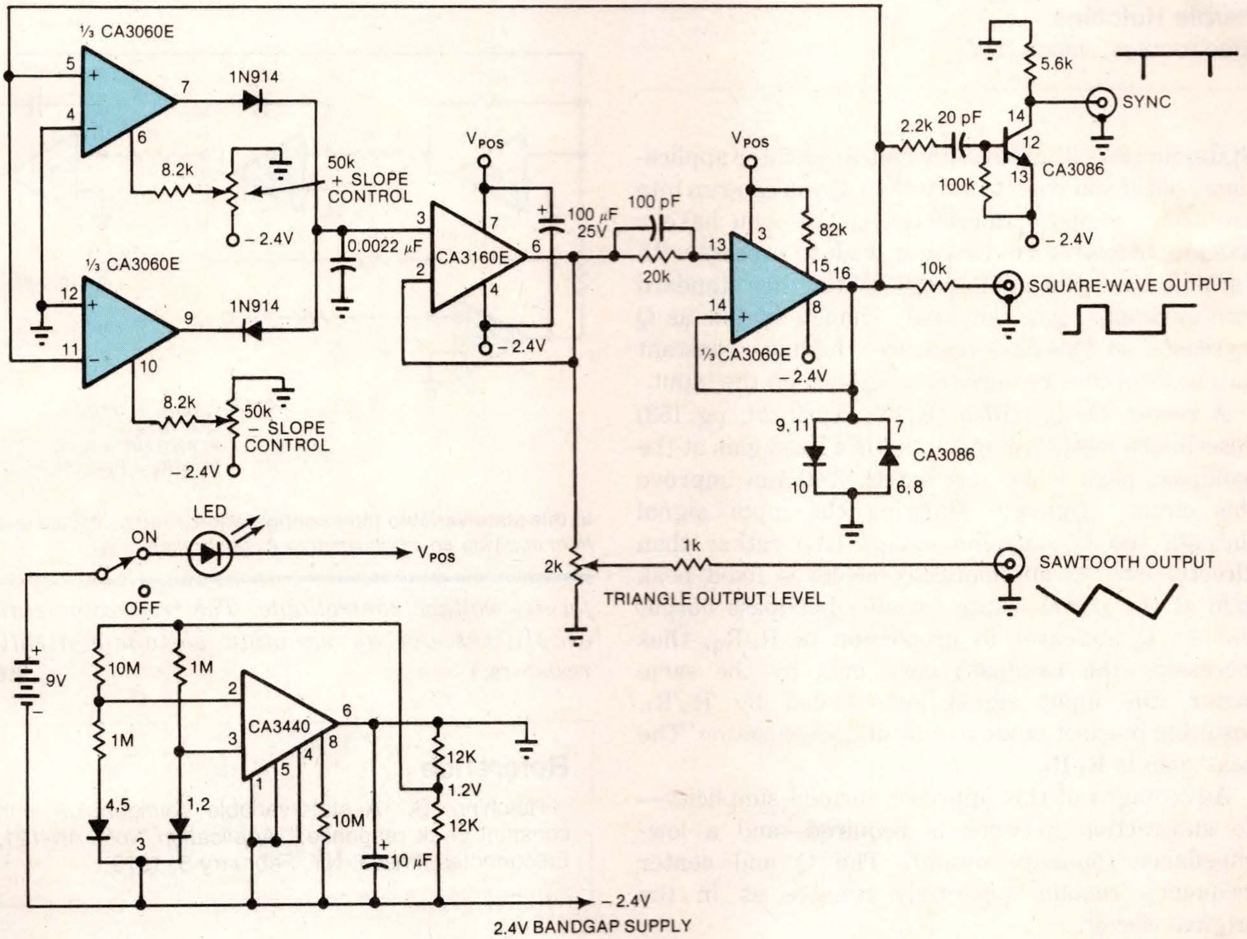
OTA function generator achieves wide range

Hal Wittlinger
RCA Solid State Div, Somerville, NJ

You can use two operational transconductance amplifiers (OTAs) to form a function generator (**figure**). In this circuit, the two OTAs, which make excellent controllable current sources, connect to a capacitor —one as a current source that causes capacitor voltage to linearly increase and the other as a sink that linearly ramps the voltage down. The ramp time spans a 1,000,000:1 range; a 0.0022-μF capacitor furnishes 20-μsec to 20-sec timing. Thus, the OTA-based circuit can generate a sawtooth (or triangle) waveform with independently adjustable rise and fall times within this range.

The waveform-generator circuit is designed around the CA3060E, a triple transconductance amplifier. Two amplifiers serve as the switched current generators, allowing direct integration on the 0.0022-μF capacitor. A 50-kΩ bias-current control potentiometer sets the output current of each current generator at approximately 2.5 times the bias current.

The resulting waveform is buffered by a high-impedance BiMOS operational amplifier (CA3160E) connected as a voltage follower. This BiMOS amplifi-



Operational transconductance amplifiers *give this waveform generator a 1,000,000:1 range. Two of the OTAs act as switched current generators controlled by the third, allowing direct integration of their two outputs by a 0.0022-μF film or mica capacitor.*

er drives both the 2-kΩ output attenuator and the following hysteresis switch (comparator). The third CA3060E amplifier serves as a noninverting switch that drives the inputs of its two mates.

Two transistors of a CA3086 array, connected as diodes, serve as output limiters for the symmetrical output of the hysteresis switch; output excursion is approximately ±0.7V. Another CA3086 transistor serves as a synchronization pulse shaper.

A micropower bandgap-reference power supply comprising a CA3440 and two additional diode-connected transistors from the CA3086 keeps the output frequency stable with changes in battery voltage. The nominal 1.2V bandgap reference is scaled up by the two 12-kΩ resistors across the output. Total supply current for this reference, exclusive of the load current, is less than 15 μA. An artificial ground formed at the output of this reference supply ensures a symmetrical swing for both the sawtooth and pulse outputs.

The waveform generator consumes 3 to 11 mA from a 9V battery. The LED serves as voltage-dropping diode, pilot light and low-battery indicator. Life of the MN1604 9V battery should be approximately 100 hrs. **EDN**

To Vote For This Design, Circle No 450

Filter's gain is independent of Q

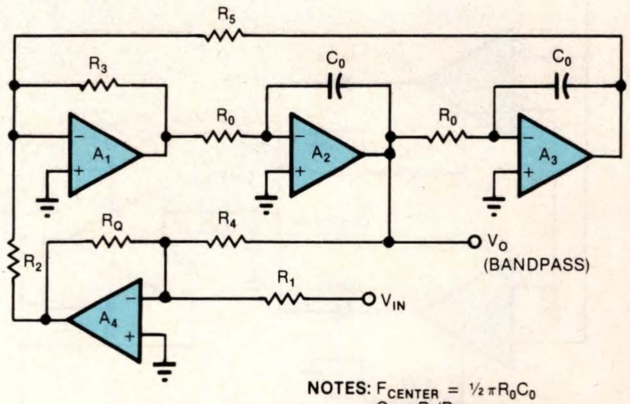
Bernie Hutchins
Electronotes, Ithaca, NY

State-variable filters readily suit fixed-filter applications, but if you wish to vary their Q you can run into problems. Suppose, for instance, that you have a fixed input waveform that you wish to process with variable-bandwidth filtering. With the standard configurations, you can easily change Q, but as Q increases, so does peak response. Holding a constant output level thus requires cutting back on the input.

A recent Design Idea (EDN, April 28, pg 153) described a method of maintaining a fixed gain at the bandpass peak while varying Q. You can improve this circuit (**figure**): Applying the input signal through the Q-controlling stage (A_4) rather than directly into A_1 automatically achieves fixed peak gain at the normal state-variable bandpass output V_O. As Q increases in proportion to R_4/R_Q, thus increasing the bandpass peak gain by the same factor, the input signal gets scaled by R_Q/R_1, resulting in exact input-to-output compensation. The peak gain is R_4/R_1.

Advantages of this approach include simplicity—no subtraction network is required—and a low-impedance (op-amp) output. The Q and center frequency remain separately tunable as in the original circuit.

(Ed Note: The state-variable filter is particularly interesting to electronic-music enthusiasts. Replacing the two resistors labeled R_0, which set f_{CENTER}, with CA3080 transconductance amplifiers makes f_{CENTER} voltage controllable. The transconductance amplifiers act as variable voltage-controlled resistors.) **EDN**



NOTES: $F_{CENTER} = \frac{1}{2}\pi R_0 C_0$
$Q = R_4/R_Q$
PEAK GAIN $= R_4/R_1$
$R_2 = R_3 = R_5 \sim 100k$

In this state-variable-filter configuration, *fixed peak gain results from applying an input signal to A_4 rather than to A_1.*

Reference

Hutchins, B, "A state-variable configuration with constant peak response," *Application Note AN-121*, Electronotes, Ithaca, NY, February 5, 1979.

To Vote For This Design, Circle No 451

Continued on pg 169

TELEDYNE SEMICONDUCTOR

Teledyne Semiconductor Selector Guide

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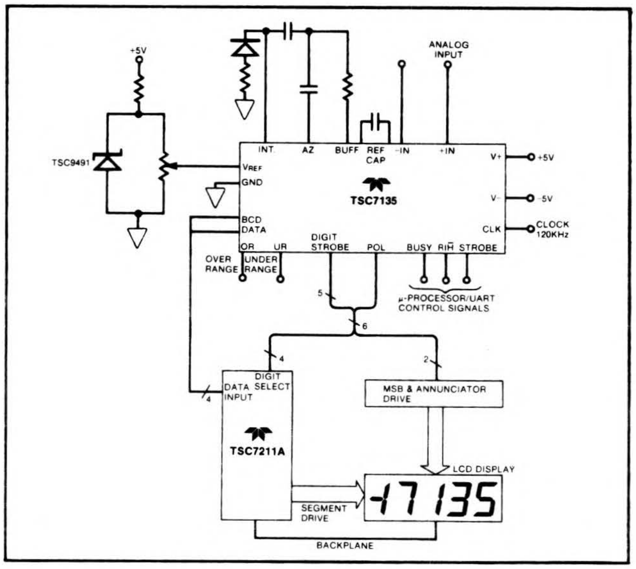
- Low Power Dissipation . . . 10mW

SYSTEM APPLICATION



Part No.	Package	Resolution	Conversion Rate	Input Noise
TSC7135 CJI	28-Pin CerDIP	4½-Digits	3 Readings/Sec	10μVp-p
TSC7135 CPI	28-Pin Plastic	4½-Digits	3 Readings/Sec	10μVp-p

4-Digit, Seven Segment LCD and LED Decoder/Drivers

TSC7211A (LCD Drive)
TSC700A (LED Drive)
TSC7212A (LED Drive)

TSC7211A Features

- On-Chip Oscillator Generates Backplane Drive Frequency
- Wide Supply Voltage Operation . . . 3V to 6V
- Code B Output Format

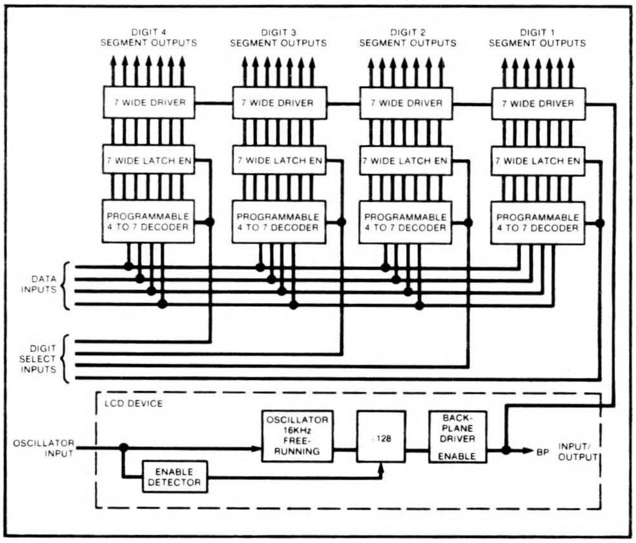
TSC700A Features

- Guaranteed 11mA Minimum LED Segment Current
- Brightness Control

TSC7212A Features

- Guaranteed 5mA Minimum LED Segment Current
- Brightness Control

FUNCTIONAL DIAGRAM



Part No.	Package	Output Drive	LED Segment Drive Current	Output Code
TSC7211 AIPL	40 Pin Plastic Dip	LCD	NA	0-9,E,L,H,P, (blank)
TSC700 AIJL	40 Pin CerDIP	LED	11mA Minimum	0-9,E,L,H,P, (blank)
TSC700 AMJL	40 Pin CerDIP	LED	11mA Minimum	0-9,E,L,H,P, (blank)
TSC700 AMJL/883	40 Pin CerDIP	LED	11mA Minimum	0-9,E,L,H,P, (blank)
TSC7112 AIPL	40 Pin Plastic Dip	LED	5mA Minimum	0-9,E,L,H,P, (blank)

3½-Digit LCD Drive Analog-to-Digital Converters

TSC7106
TSC7116
TSC7126

Family Features

- Auto-Zero
- True Polarity at Zero for Precise Null Detection
- 1 pA Input Current
- Direct Display Drive—No External Components Required
- Low Noise—Less than 15μVp-p
- On-Chip Clock and Reference

TSC7106 Features

- Power Dissipation Typically Less than 10 mW
- True Differential Input and Reference
- No Other Active Circuits Required

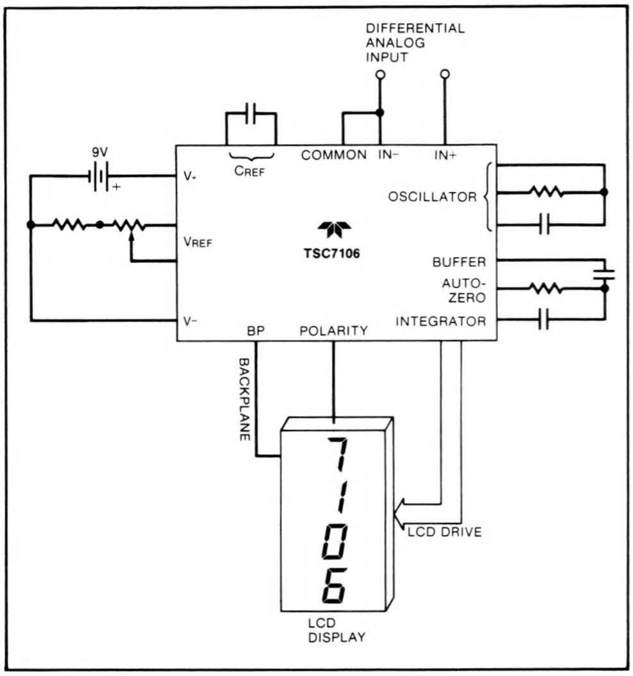
TSC7116 Features

- Hold Function for Indefinite Display Hold
- Differential Analog Input
- Low Noise—Less than 15μVp-p
- On-Chip Clock and Reference
- Power Dissipation Typically Less than 10mW
- No Other Active Circuits Required

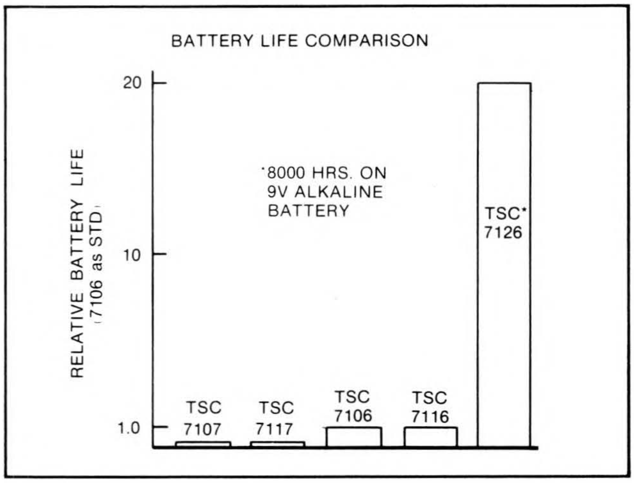
TSC7126 Features

- 8000 Hours Typical 9 Volt Battery Life
- Pin Compatible with 7106
- Power Dissipation Typically Less than 1mW
- True Differential Input and Reference

FUNCTIONAL DIAGRAM



BATTERY LIFE COMPARISON



Part No.	Package	Pin Layout	Display Hold Function	Power Dissipation	Input Sensitivity	Differential Reference
TSC7106 CDL	40 Pin Ceramic Dip	Normal	No	10mW	10μV	Yes
TSC7106 CJL	40 Pin CerDIP	Normal	No	10mW	10μV	Yes
TSC7106 CPL	40 Pin Plastic Dip	Normal	No	10mW	10μV	Yes
TSC7106 RCPL	40 Pin Plastic Dip	Reversed	No	10mW	10μV	Yes
TSC7126 CDL	40 Pin Ceramic Dip	Normal	No	1mW	10μV	Yes
TSC7126 CJL	40 Pin CerDIP	Normal	No	1mW	10μV	Yes
TSC7126 CPL	40 Pin Plastic Dip	Normal	No	1mW	10μV	Yes
TSC7116 CDL	40 Pin Ceramic Dip	Normal	Yes	10mW	10μV	No
TSC7116 CJL	40 Pin CerDIP	Normal	Yes	10mW	10μV	No
TSC7116 CPL	40 Pin Plastic Dip	Normal	Yes	10mW	10μV	No

3½-Digit LED Drive Analog-to-Digital Converter

TSC7107
TSC7117

Family Features

- Auto-Zero, Auto-Polarity
- True Polarity at Zero for Precise Null Detection
- 1 pA Input Current
- Direct Display Drive—No External Components Required
- Low Noise—Less than 15μVp-p
- On-Chip Clock and Reference
- Bright Display for Easy Reading
- Ratiometric Reading

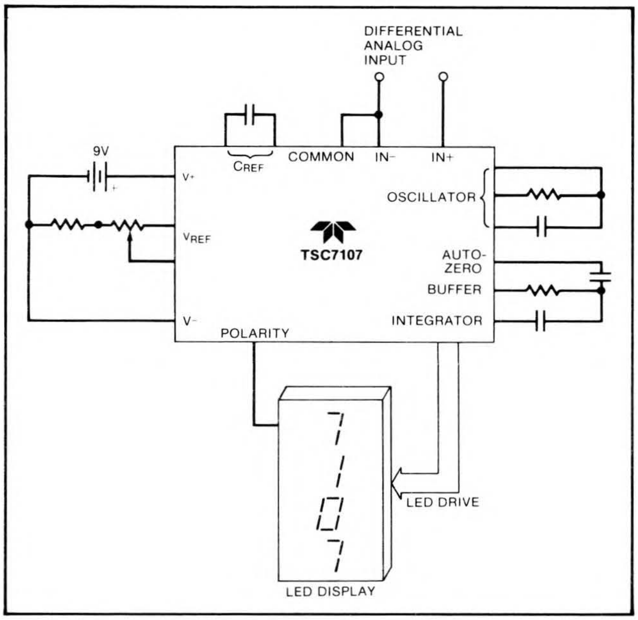
TSC7107 Features

- True Differential Input and Reference

TSC7117 Features

- Hold Function for Indefinite Display Hold
- Differential Input

FUNCTIONAL DIAGRAM



Part No.	Package	Pin Layout	Display Hold Function	Input Sensitivity	Differential Reference
TSC7107 CDL	40 Pin Ceramic Dip	Normal	No	10μV	Yes
TSC7107 CJL	40 Pin CerDIP	Normal	No	10μV	Yes
TSC7107 CPL	40 Pin Plastic Dip	Normal	No	10μV	Yes
TSC7107 RCPL	40 Pin Plastic Dip	Reversed	No	10μV	Yes
TSC7117 CDL	40 Pin Ceramic Dip	Normal	Yes	10μV	No
TSC7117 CJL	40 Pin CerDIP	Normal	Yes	10μV	No
TSC7117 CPL	40 Pin Plastic Dip	Normal	Yes	10μV	No

3½-Digit Multiplexed BCD Output Analog-to-Digital Converters

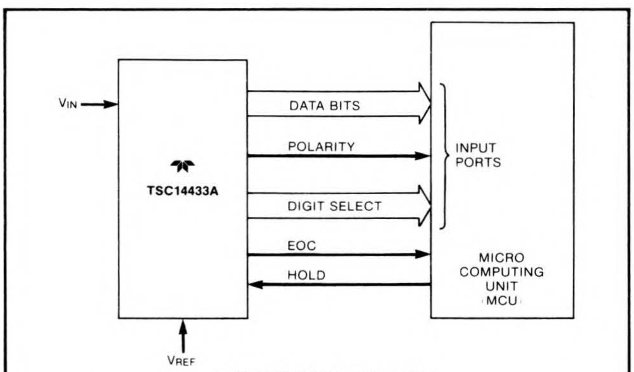
TSC14433
TSC14433A

TSC14433 Features

- Accuracy: ±0.05% of Reading ±1 Count
- Auto-Polarity and Auto-Zero
- On-Chip System Clock or External Clock
- Wide Supply Range: e.g., ±4.5V to ±8.0V
- Overrange and Underrange Signals
- Operates with LED and LCD Displays

TSC14433A Features

Same as 14433 Plus:
- Rollover Error < 1 Count
- Lower Power Consumption . . . 4mW



MICROPROCESSOR INTERFACE

Part No.*	Package	Conversion Rate	Rollover Error	Power Dissipation
TSC14433 CJ	24 Pin Plastic Dip	25 conv./sec	—	8mW
TSC14433A CJ	24 Pin Plastic Dip	25 conv./sec	1 count	4mW

*Also available in Ceramic and CerDIP Packages.

13-Bit Analog-to-Digital Converter

TSC7109

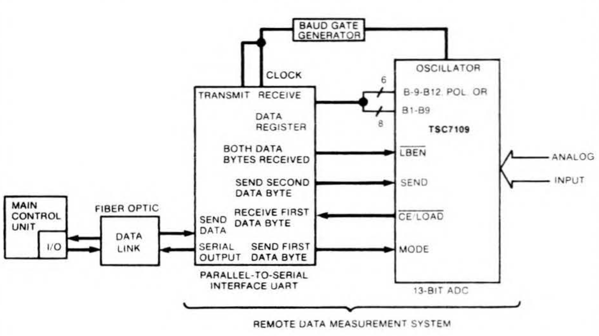
Features

- 12-Bit Plus Sign Integrating ADC
- Overrange and Polarity Bit
- Sign Magnitude Code Format
- Single or Two Byte μP Bus Interface
- Three-State Outputs Interface to 8/16-Bit Processors
- UART Control Signals
- Differential Analog Input and Reference
- Auto-Zero Cycle Eliminates Zero Potentiometer
- On-Chip Oscillator
- Automatic 60 Hz Noise Rejection
- Ratiometric Conversion
- Low Input Noise—15μVp-p
- Low Power—20mW

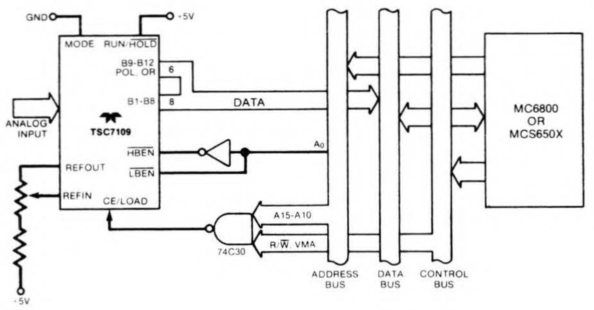
TSC7109 VS. SUCCESSIVE APPROXIMATION ADC

Preferred Characteristics	TSC7109 Integrating ADC	12-Bit SAR ADC
μP - Compatible	√	Some
UART - Interface	√	
High Impedance Input	√	
Internal Reference	√	Some Hybrids
60 Hz Noise Rejection	√	
Noise Averaging	√	
High Speed		√
Good Sensitivity	√	
Internal Clock	√	Some Hybrids
13-Bit Resolution	√	
2's Complement Coding		√ (or Offset Binary)
No Zero Trim Needed	√	
Low Power	√	
Low Cost IC	√	
S/H Amplifier Not Needed	√	

"HANDSHAKE" SERIAL DATA TRANSMISSION



PARALLEL BUS INTERFACE



Part No.	Package	Temp. Range	Input Bias Current Over Temperature
TSC7109 MDL	40 Pin Ceramic Dip	−55° to +125°C	5nA
TSC7109 MJL	40 Pin CerDIP	−55° to +125°C	5nA
TSC7109 BMDL	40 Pin CerDIP	−55° to +125°C	10nA
TSC7109 MDL/883	40 Pin Ceramic Dip	−55° to +125°C	5nA
TSC7109 MJL/883	40 Pin CerDIP	−55° to +125°C	5nA
TSC7109 BMJL/883	40 Pin CerDIP	−55° to +125°C	10nA
TSC7109 IDL	40 Pin Ceramic Dip	−25° to +85°C	250pA
TSC7109 IJL	40 Pin CerDIP	−25° to +85°C	250pA
TSC7109 CPL	40 Pin Plastic Dip	0°C to +70°C	100pA
TSC7109 BIJL	40 Pin CerDIP	−25° to +85°C	500pA
TSC7109 BCPL	40 Pin Plastic Dip	0°C to +70°C	500pA

8, 10, 12-Bit A/D Converters

TSC8700
TSC8701
TSC8702

Features

- High Accuracy — Up to 12-Bit Resolution with < ½ LSB Error
- Monotonic Performance
- Low Power Dissipation . . . 20mW
- Data Valid, Busy and Start Conversion Pins
- Strobed or Free Running Conversion
- Infinite Input Voltage Range—Any Positive Voltage Can Be Applied Via a Scaling Resistor

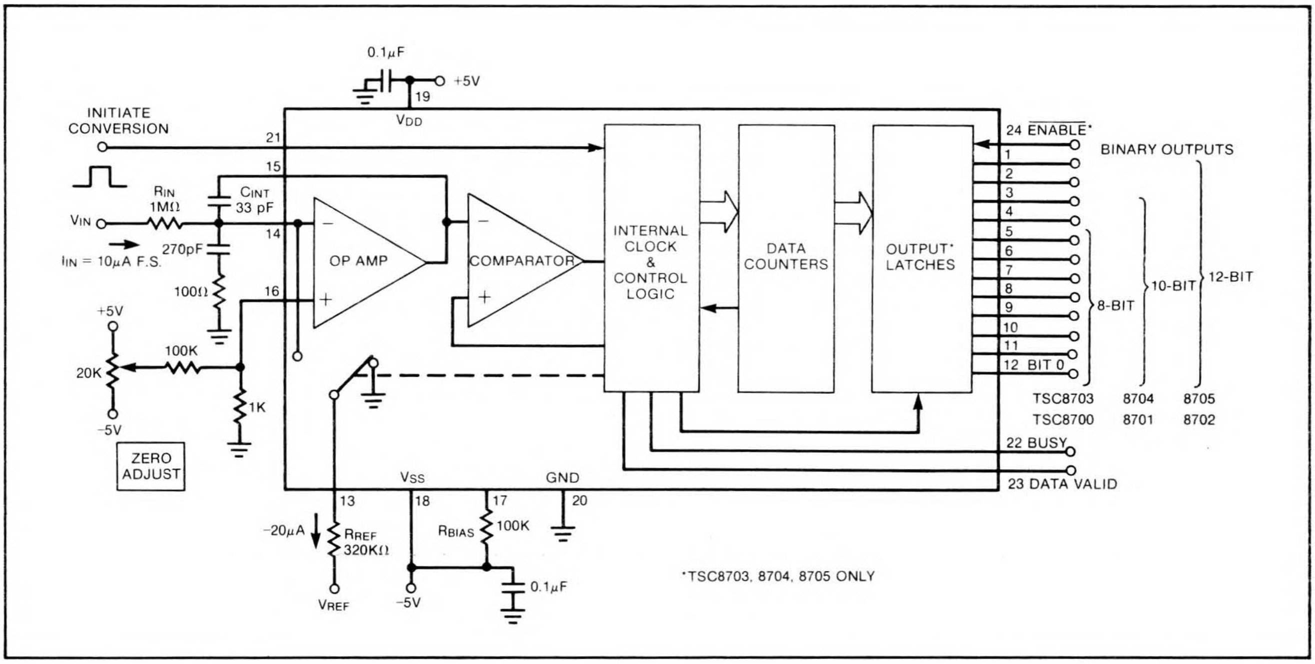
8, 10, 12-Bit Binary A/D Converters with Three-State Outputs

TSC8703
TSC8704
TSC8705

Features:

- Microprocessor Compatible
- High Accuracy — Up to 12-Bit Resolution with < ½ LSB Error
- Monotonic Performance
- Low Power Dissipation — 20mW
- Latched Parallel Binary Outputs
- Data Valid, Busy and Start Control Pins
- Strobed or Free Running Conversion
- Infinite Input Range—Any Positive Voltage Can Be Applied Via a Scaling Resistor

FUNCTIONAL DIAGRAM



Part No.	Package	Temperature Range	Resolution	Conversion Spread
TSC8700 CN	24 Pin Ceramic Dip	−40° C to +85° C	8-Bit	1.8mS
TSC8700 CJ	24 Pin Plastic Dip	0° C to +70° C	8-Bit	1.8mS
TSC8700 CN	24 Pin Ceramic Dip	−40° C to +85° C	10-Bit	6.0mS
TSC8700 CJ	24 Pin Plastic Dip	0° C to +70° C	10-Bit	6.0mS
TSC8700 CN	24 Pin Ceramic Dip	−40° C to +70° C	12-Bit	24mS
TSC8703 BN	24 Pin Ceramic Dip	−55° C to +125° C	8-Bit	1.8mS
TSC8703 CN	24 Pin Ceramic Dip	−40° C to +85° C	8-Bit	1.8mS
TSC8703 CJ	24 Pin Plastic Dip	0° C to +70° C	8-Bit	1.8mS
TSC8704 BN	24 Pin Ceramic Dip	−55° C to +125° C	10-Bit	6mS
TSC8704 CN	24 Pin Ceramic Dip	−40° C to +85° C	10-Bit	6mS
TSC8704 CJ	24 Pin Plastic Dip	0° C to +70° C	10-Bit	6mS
TSC8705 BN	24 Pin Ceramic Dip	−55° C to +125° C	12-Bit	24mS
TSC8705 CJ	24 Pin Plastic Dip	0° C to +70° C	12-Bit	24mS

Monolithic Voltage References/ Temperature Transducers

TSC9491
TSC9495
TSC9496

TSC9491 Features

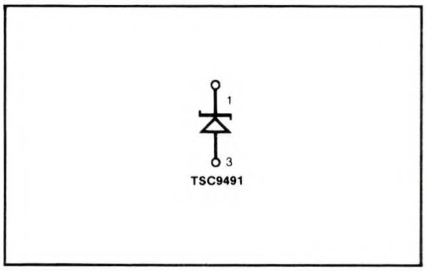
- +1.22 Volt Output
- Low Supply Current: 50μA
- Small TO-18 or TO-92 Package
- Reference for TSC7106/7126/7109 Converters

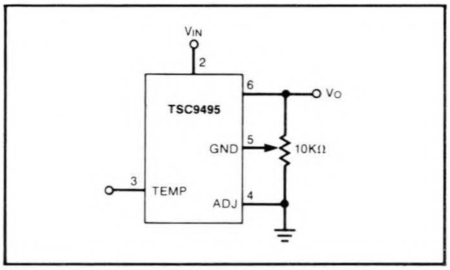
TSC9495 Features

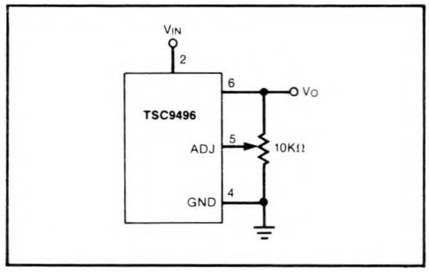
- +5.0 Volt Output
- Choice of Tolerance: 0.3% and 1%
- Temp. Output Measures Temperature
- Low Noise: 15 μVpp Max.
- Replaces REF-02

TSC9496 Features

- +10 Volt Output
- Choice of Tolerance: 0.3% and 1%
- Low Noise: 30 μVpp Max.
- Replaces REF-01







Part No.	Package	Temperature Range	Output Voltage	Max. Temp. Coefficient	Accuracy
TSC9491 AJ	TO-92	0°C to +70°C	1.22V	50ppm/°C	2.5%
TSC9491 BJ	TO-92	0°C to +70°C	1.22V	100ppm/°C	2.5%
TSC9495 CE	TO-99	0°C to +70°C	5.000V	65ppm/°C	1.0%
TSC9495 CJ	8 Pin Plastic Dip	0°C to +70°C	5.000V	65ppm/°C	1.0%
TSC9495 EE	TO-99	0°C to +70°C	5.000V	8.5ppm/°C	0.3%
TSC9496 CE	TO-99	0°C to +70°C	10.000V	65ppm/°C	1.0%
TSC9496 CJ	8 Pin Plastic Dip	0°C to +70°C	10.000V	65ppm/°C	1.0%
TSC9496 EE	TO-99	0°C to +70°C	10.000V	8.5ppm/°C	0.3%

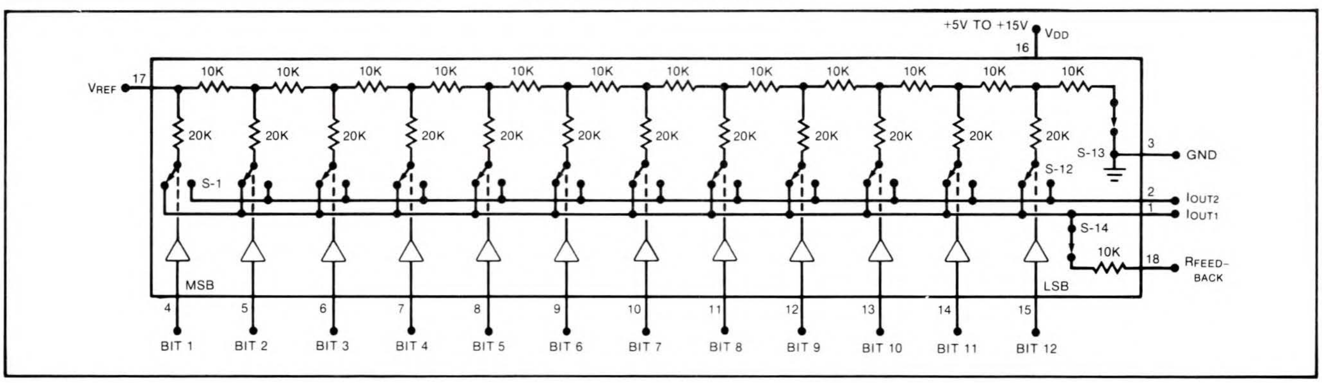
Monolithic CMOS Converters Digital-to-Analog

TSC8640
TSC8641

Features

- 12-Bit Linearity (0.01% Achieved Without Laser Trimming)
- 2ppm/°C Max Gain Error Tempco
- Full Four Quadrant Multiplication
- Low Power CMOS, <30mW
- TTL/CMOS Compatible Inputs
- Low Feedthrough Error
- Compensated Feedback Resistor
- Low Cost
- Direct Replacement for AD7521 and AD7541

FUNCTIONAL DIAGRAM



Part No.	Package	Temperature Range	Non-Linearity	Resolution
TSC8640 BN	18 Pin Ceramic Dip	−55°C to +125°C	0.024%	12-Bits
TSC8640 CN	18 Pin Ceramic Dip	−25°C to +85°C	0.024%	12-Bits
TSC8640 CJ	18 Pin Plastic Dip	0°C to +70°C	0.024%	12-Bits
TSC8641 BN	18 Pin Ceramic Dip	−55°C to +125°C	0.012%	12-Bits
TSC8641 CN	18 Pin Ceramic Dip	−25°C to +85°C	0.012%	12-Bits
TSC8641 CJ	18 Pin Plastic Dip	0°C to +70°C	0.012%	12-Bits

Voltage-To-Frequency/ Frequency-To-Voltage Converters

TSC9400
TSC9401
TSC9402

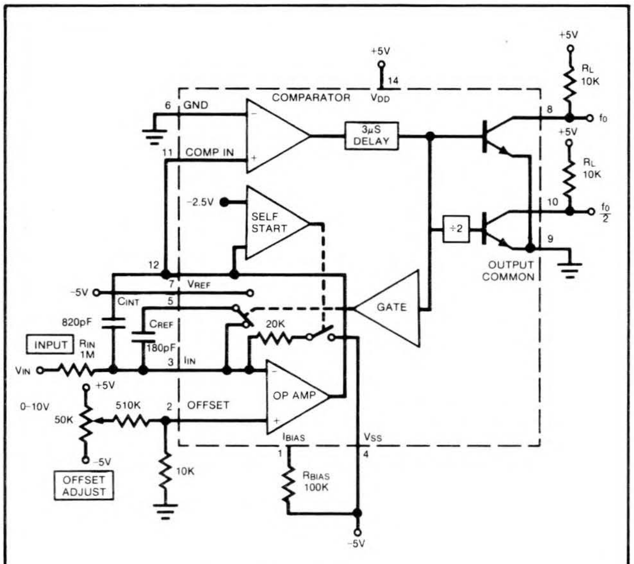
Features

- 1Hz to 100KHz Operation
- ±25ppm/°C Typ. Gain Temperature Stability
- Open Collector Outputs
- Pulse and Square Wave Outputs
- Programmable Scale Factor
- Current Input Accommodates Large Signal Inputs
- Low-power Dissipation . . . 27mW

Frequency-to-Voltage

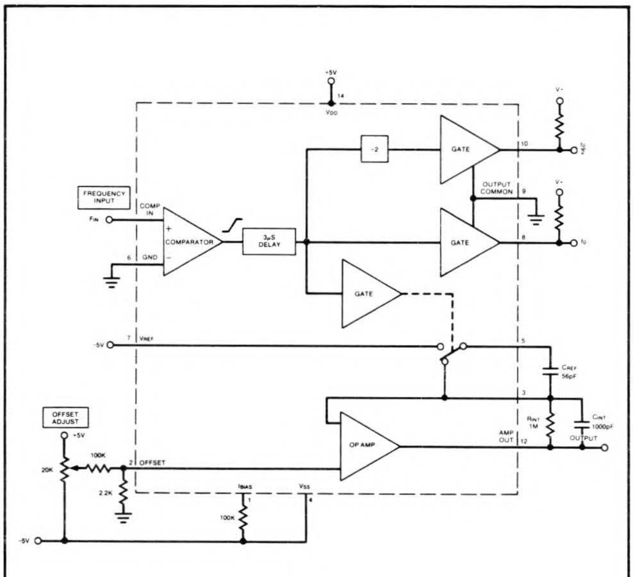
- DC to 100KHz Operation
- Operational Amplifier Output
- Programmable Scale Factor
- High Input Impedance (>10MΩ)

V/F CIRCUIT CONNECTION



10Hz to 10KHz V/F Converter

F/V CIRCUIT CONNECTION



DC to 10KHz V/F Converter

Part No.	Package	Temperature Range	Non-Linearity	Gain Temperature Drift
TSC9400 CJ	14 Pin Plastic Dip	0°C to +70°C	0.05%	40ppm/°C
TSC9400 CN	14 Pin Ceramic Dip	−40°C to +85°C	0.05%	40ppm/°C
TSC9400 CL	14 Pin CerDIP	−40°C to +85°C	0.05%	40ppm/°C
TSC9401 CJ	14 Pin Plastic Dip	0°C to +70°C	0.01%	40ppm/°C
TSC9401 CN	14 Pin Ceramic Dip	−40°C to +85°C	0.01%	40ppm/°C
TSC9401 CL	14 Pin CerDIP	−40°C to +85°C	0.01%	40ppm/°C
TSC9401 CJ	14 Pin Plastic Dip	0°C to +70°C	0.25%	100ppm/°C
TSC9402 CL	14 Pin CerDIP	−40°C to +85°C	0.25%	100ppm/°C

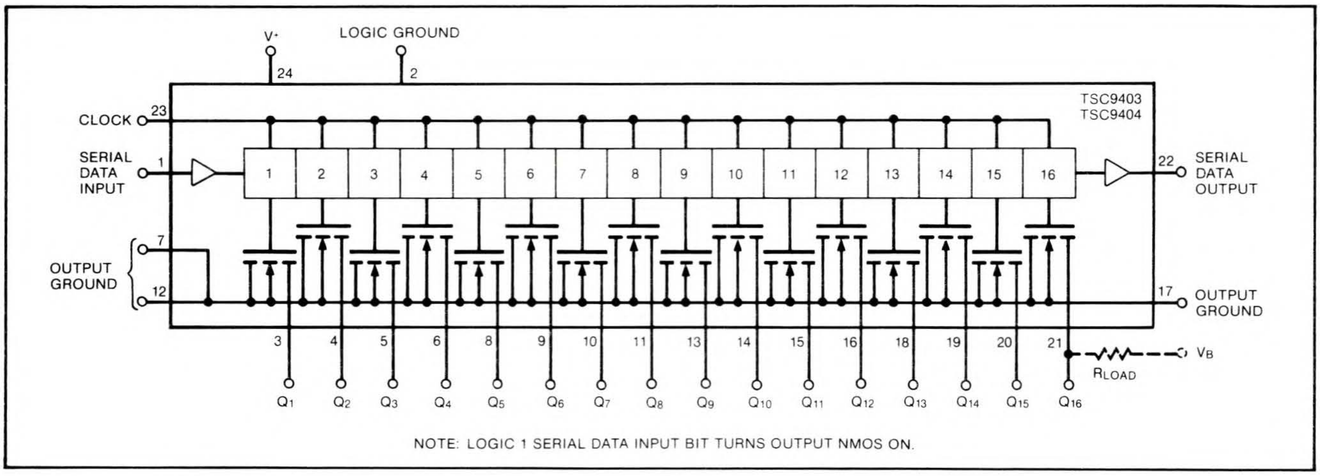
Serial Input/16-Bit Parallel Output Peripheral Driver

TSC9403
TSC9404

Features
- High Voltage Outputs: 20V (TSC9403), 15V (TSC9404)
- High Output Current Sink Capability: 60mA @ Vsat = 0.5V
- Low Standby Power: 20mW Maximum
- High Speed Operation: 5.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

Applications
- High Current Voltage μ-Processor Serial Port Expander
- LED Bar Graph Driver
- Thermal Printhead Driver
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

FUNCTIONAL DIAGRAM

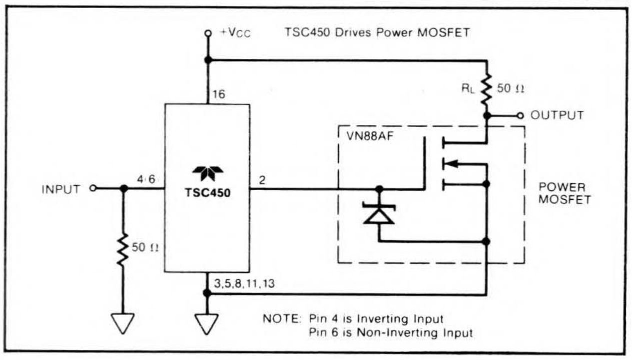


Part No.	Package	Temperature Range	Output Voltage	Rate Clock
TSC9403 CJ	24-Pin Plastic Dip	0°C to +70°C	20V	5.0MHz
TSC9403 IL	24-Pin CerDIP	−25°C to +85°C	20V	5.0MHz
TSC9404 CJ	24-Pin Plastic Dip	0°C to +70°C	15V	5.0MHz
TSC9404 IL	24-Pin CerDIP	−25°C to +85°C	15V	5.0MHz

Dual Power MOSFET Driver

TSC450

Features
- Dual Device for High Packing Density
- User Selectable Inverting on Non-Inverting Operation
- Single Supply Operation
- TTL-Compatible Inputs
- High Voltage Outputs .... V_{CC}-1V
- High Output Sink Current 12mA
- High Output Source Current 6mA
- Fast Switching 125nS
- Available with MIL-STD-883B Processing



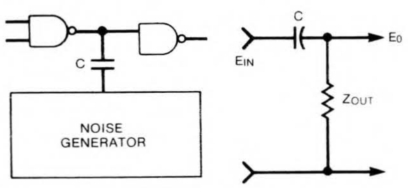
Part No.	Package	Temperature Range	Supply Voltage
TSC450 AIJE	16-Pin CerDIP	−25°C to +85°C	15V
TSC450 ACPE	16-Pin Plastic Dip	0°C to +70°C	15V
TSC450 BIJE	16-Pin CerDIP	−25°C to +85°C	12V
TSC450 BCPE	16-Pin Plastic Dip	0°C to +70°C	12V
TSC450 AMJE	16-Pin CerDIP	−55°C to +125°C	15V
TSC450 BMJE	16-Pin CerDIP	−55°C to +125°C	12V
TSC450 AMJE/883	16-Pin CerDIP	−55°C to +125°C	15V
TSC450 BMJE/883	16-Pin CerDIP	−55°C to +125°C	12V

Series 300 Bipolar Logic Interface Products

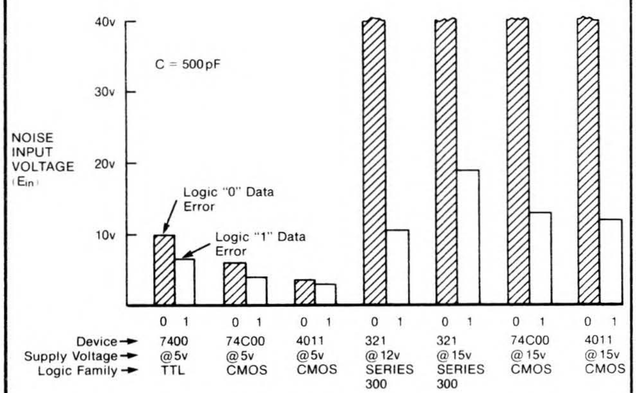
Family Features

- High-Noise Immunity . . . 3.5V to 6.5V
- Rugged Bipolar Construction
- Immunity to Electrostatic Destruction
- Output Current Drive to 250mA
- Wide Supply Voltage Operation . . . 11V to 16V
- Active and Passive Pull-Up Output Stages

SERIES 300 LOGIC OFFERS HIGH-NOISE SPIKE IMMUNITY



ELECTRICAL NOISE MODEL

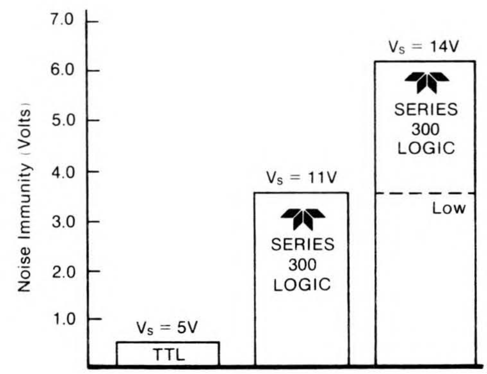


NOISE IMMUNITY TEST RESULTS

Typical High Noise Environments

Copy Machines
Facsimile Machines
Automotive Test Equipment
Coin Changers
Credit Card Vending Machines
Alarm Systems
Traffic Controllers
Gasoline Pumps
Conveyor Belt Controllers
Missile Fire Controllers
Welding Equipment
Robots
Radar Systems
Numerically Controlled Machine Tools
Chemical Plants
Energy Management Systems
Motor Control Systems

NOISE IMMUNITY VS. LOGIC FAMILY

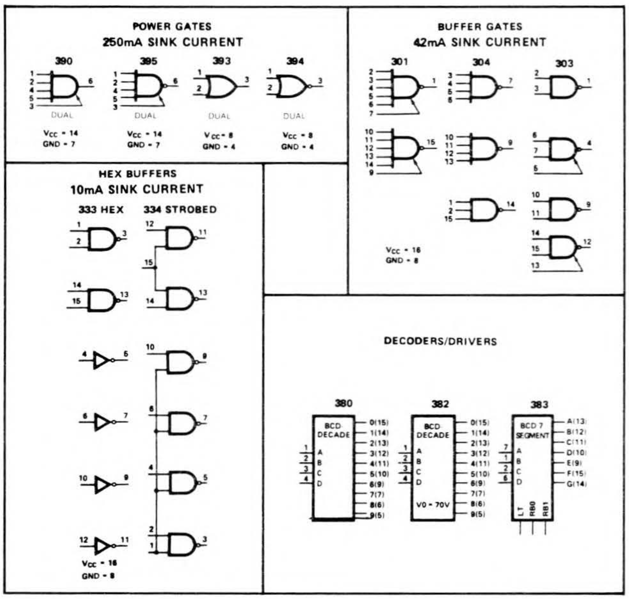


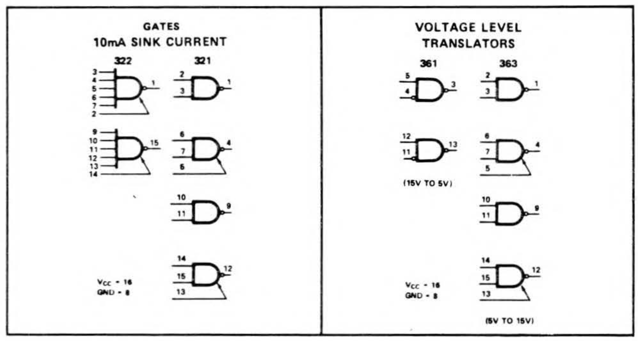
Series 300 Product Guide

Features

- Operation on 11V to 16V Power Supplies
- Low Output Impedance: 3Ω
- High Sink and Source Current: Up to 250mA
- CMOS Compatible Inputs (When operating on 11V to 16V power supplies)
- Rugged Bipolar Construction
- 1 MHz Limited Band Width for High Frequency Noise Rejection
- Proven High Reliability

Most Popular Series 300 Products





Additional Products:
- Timers
- Digital Multiplexers
- One Shots
- Four Bit Comparators
- Decade Counters
- Up/Down Counters
- Quad D Flip Flops
- AND-OR-Invert Gates
- Dual, Triple and Quad Gates
- Send for Full Product Line Catalog

Field Effect Transistors

The following four pages provide principle specifications on all devices in Teledyne's broad JFET product line. Arranged by geometry for easy comparison and choice between similar devices, it simplifies selection of the ideal device for a given application or performance requirement.

1127

General-Purpose Amplifier and Switch

Metal Package

Device	g_{fs} mmhos Min.	g_{fs} mmhos Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$r_{DS(ON)}$ Ω Max.	NF/$\bar{e}_n$ dB Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	Package (*available in plastic)
2N3823	3.5	6.5	500	—	8	—		4	20	30	6	2	TO-72
2N3822	3.0	6.5	100	—	6	—	200nV/$\sqrt{Hz}$	2	10	50	6	3	TO-72
2N4223	3.0	7.0	250	0.1	8	—	5	3	18	30	6	2	TO-72*
2N3967	2.5	—	100	2	5	400	1.5	2.5	10	30	5	1.3	TO-72
2N3968	2.0	—	100	—	3	700	1.5	1	5	30	5	1.3	TO-72
2N4224	2.0	7.5	500	0.1	8	—	—	2	20	30	6	2	TO-72
2N5556	1.5	6.5	100	0.2	4	—	20 nV/$\sqrt{Hz}$	0.5	2.5	30	6	3	TO-72
2N5557	1.5	6.5	100	0.8	5	—	20 nV/$\sqrt{Hz}$	2	5	30	6	3	TO-72
2N5558	1.5	6.5	100	1.5	6	—	20 nV/$\sqrt{Hz}$	4	10	30	6	3	TO-72
2N3969	1.3	—	100	—	1.7	—	1.5	0.4	2	30	5	1.3	TO-72
2N3824	—	—	100	—	8	250	—	—	—	50	6	3	TO-72
2N3966	—	—	100	4	6	220	—	2	—	30	6	1.5	TO-72
2N3821	1.5	4.5	100	—	4	—	200 nV/$\sqrt{Hz}$	0.5	5	50	6	3	TO-72

(cont.)

1127
General-Purpose Amplifier and Switch (cont.)

Plastic Package

Device	g_{fs} mmhos Min.	g_{fs} mmhos Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$r_{DS(ON)}$ Ω Max.	NF/$\bar{e}_n$ dB Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	Package (*available in plastic)
BC264D	4.0	—	10000	0.5	—	—	2	7	12	30	4	1.2	TO-92RR
2N5949	3.5	7.5	1000	3	7	200	5	12	18	30	6	2	TO-92RR
2N5950	3.5	7.5	1000	2.5	6	210	5	10	15	30	6	2	TO-92RR
2N5951	3.5	6.5	1000	2	5	250	5	7	13	30	6	2	TO-92RR
BC264C	3.5	—	10000	0.5	—	—	2	5	8	30	4	1.2	TO-92RR
BC264B	3.0	—	10000	0.5	—	—	2	3.5	6.5	30	4	1.2	TO-92RR
BC264	2.5	—	10000	0.5	—		2	2	12	30	4	1.2	TO-92RR
BC264A	2.5	—	10000	0.5	—	—	2	2	4.5	30	4	1.2	TO-92RR
2N5952	2.0	6.5	1000	1.3	3.5	300	5	4	8	30	6	2	TO-92RR
2N5953	2.0	6.5	1000	0.8	3	375	5	2.5	5	30	6	2	TO-92RR
J5163	1.8	—	10000	0.4	8	500	3	1	40	25	20	5	TO-92
J103	1.5	—	500	2	10	650	—	4	20	30	3	3	TO-92
J102	1.0	—	500	0.8	4	1,200	—	0.9	4.5	30	8	3	TO-92
J100	0.5	—	500	0.3	10	3,000	—	0.2	20	30	8	3	TO-92
J101	0.5	—	500	0.3	1.5	3,000	—	0.2	1	30	8	3	TO-92

1134
GP Low-Noise Amplifier—68 nV/$\sqrt{Hz}$ @ 1 KHz

Device	g_{fs} mmhos Min.	g_{fs} mmhos Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	NF/$\bar{e}_n$ dB Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	Package (*available in plastic)
2N4339	0.8	2.4	0.1	0.6	1.8	68 nV/$\sqrt{Hz}$	0.5	1.5	50	7	3	TO-18*
2N4338	0.6	1.8	0.1	0.3	1	68 nV/$\sqrt{Hz}$	0.2	0.6	50	7	3	TO-18*
J4303	2	—	1	—	6	2	4	10	30	6	3	TO-92
J4302	1	—	1	—	4	2	0.5	5	30	6	3	TO-92
J4304	1	—	1	—	10	3	0.5	15	30	6	3	TO-92

1135
VHF RF Amplifier—400 MHz

Metal Package

Device	g_{fs} mmhos Min.	g_{fs} mmhos Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	N.F. @ 400MHz dB Max.	Package (*Available in Plastic)
2N4416	4.5	7.5	100	—	6	5	15	30	4	0.8	4	TO-72*
BFW10	3.5	6.5	100	—	8	8	20	30	5	0.8	2.5	TO-72
BFW11	3.0	6.5	100	—	6	4	10	30	4	0.8	2.5	TO-72
BFW61	2.0	6.5	100	—	8	2	20	25	6	2.0	—	TO-72

Plastic Package

Device	g_{fs} mmhos Min.	g_{fs} mmhos Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	N.F. @ 400MHz dB Max.	Package (*Available in Plastic)
BF256	4.5	5	5	0.5	7.5	3	18	30	—	—	—	TO-92RR
BF256A	4.5	5	5	0.5	7.5	3	7	30	—	—	—	TO-92RR
BF256B	4.5	5	5	0.5	7.5	6	13	30	—	—	—	TO-92RR
BF256C	4.5	5	5	0.5	7.5	11	18	3	—	—	—	TO-92RR
U1837J	4.5	10	0.25	0.5	8	4	25	30	6	2	3	TO-92RR
2N5245	4.0	—	—	1	6	5	15	30	4.5	1.2	2	TO-92RR
2N5247	4.0	—	—	1.5	8	8	24	30	4.5	1.2	(100 MHz) 4	TO-92RR
U1994J	4.0	—	0.1	—	6	5	15	30	4	1	4	TO-92
2N5486	3.5	—	—	2	6	8	20	25	5	1.2	4	TO-92
BF244	3.0	6.5	5	0.5	8	2	25	30	4	1.6	—	TO-92
BF244A	3.0	6.5	5	0.5	8	2	6.5	30	4	1.6	—	TO-92
BF244B	3.0	6.5	5	0.5	8	6	15	30	4	1.6	—	TO-92
BF244C	3.0	6.5	5	0.5	8	12	25	30	4	1.6	—	TO-92
BF245	3.0	6.5	5	0.5	8	2	25	30	4	1.6	—	TO-92R
BF245A	3.0	6.5	5	0.5	8	2	6.5	30	4	1.6	—	TO-92R
BF245B	3.0	6.5	5	0.5	8	6	15	30	4	1.6	—	TO-92RR
BF245C	3.0	6.5	5	0.5	8	12	25	30	4	1.6	—	TO-92RR
2N5485	3.0	—	1	0.5	4	4	10	10	25	1.2	2	TO-92
2N5484	2.5	—	1	0.3	3	1	5	25	5	1.2	3	TO-92
2N5246	2.5	—	1	0.5	4	1.5	7	30	4.5	1.2	4	TO-92RR
2N5670	2.5	—	2	2	8	8	20	25	7	3	2.5	TO-92
MPF102	2.0	7.5	2	—	8	2	20	25	7	3	—	TO-92
2N5459	2.0	6	1	2	8	4	16	25	7	3	—	TO-92
2N5669	1.6	—	2	1	6	4	10	25	7	3	2.5	TO-92
2N5458	1.5	5.5	1	1	7	2	9	25	7	3	—	TO-92
2N5457	1.0	5	1	0.5	6	1	5	25	7	3	—	TO-92
2N5668	1.0	—	2	0.2	4	1	5	25	7	3	2.5	TO-92
2N5555	$r_{DS(on)}$ = 150Ωmax.		1	—	10	15	—	25	5	1.2	—	TO-92
J304	—	—	0.1	2	6	5	15	30	—	—	—	TO-92
J305	—	—	0.1	0.5	3	1	8	30	—	—	—	TO-92

1136
Low-Noise Amplifier — 10 nV/$\sqrt{Hz}$ @ 100Hz

Metal Package

Device	e_n @ 10Hz Max.	N.F. dB Max.	g_{fs} mmho Min.	g_{fs} mmho Max.	I_{GSS} pA Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	BV_{GSS} V Min.	C_{iss} pF Max.	C_{rss} pF Max.	Package
2N5392	17.5 nV/$\sqrt{Hz}$	1	2	6.0	100	0.5	2.5	1	3	70	18	5	TO-18
2N5393	17.5 nV/$\sqrt{Hz}$	1	3	6.5	100	1	3	2.5	4.5	70	18	5	TO-18
2N5394	17.5 nV/$\sqrt{Hz}$	1	4	7.5	100	1	4	4	6	70	18	5	TO-18
2N5395	17.5 nV/$\sqrt{Hz}$	1	4	7.5	100	1.5	4	5.5	8	70	18	5	TO-18
2N5396	17.5 nV/$\sqrt{Hz}$	1	4	7.5	100	2	5	7.5	10	70	18	5	TO-19

1144
General-Purpose N-Channel Switch: 25-100Ω

Metal Package

Device	$r_{DS(ON)}$ Ω Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$I_{D(OFF)}$ pA Max.	C_{iss} pF Max.	C_{rss} pF Max.	BV_{GSS} V Min.	I_{DSS} mA Min.	I_{DSS} mA Max.	Package (*Available in Plastic)
2N4856	25	4	10	250	18	8	40	50	—	TO-18*
2N4859	25	4	10	250	18	8	30	50	—	TO-18*
2N3970	30	5	10	250	25	6	40	50	150	TO-18*
2N4091	30	5	10	200	16	5	40	30	—	TO-18*
2N4391	30	4	10	100	14	3.5	40	50	150	TO-18*
2N4857	40	2	6	250	18	8	40	20	100	TO-18*
2N4860	40	2	6	250	18	8	30	20	100	TO-18*
2N4092	50	2	7	200	16	5	40	15	—	TO-18*
2N3971	60	2	5	250	25	6	40	25	75	TO-18*
2N4392	60	2	5	100	14	3.5	40	25	75	TO-18*
2N4858	60	0.8	4	250	18	8	40	8	80	TO-18
2N4861	60	0.8	4	250	18	8	30	8	80	TO-18
2N4093	80	1	5	200	16	5	40	8	—	TO-18*
2N3972	100	0.5	3	250	25	6	40	5	30	TO-18*
2N4393	100	0.5	3	100	14	3.5	40	5	30	TO-18*
NF110	120	0.5	10	—	20	—	30	5	—	TO-18
NF511	120	—	10	—	20	—	20	5	—	TO-18

Plastic Package

Device	$r_{DS(ON)}$ Ω Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$I_{D(OFF)}$ pA Max.	C_{iss} pF Max.	C_{rss} pF Max.	BV_{GSS} V Min.	I_{DSS} mA Min.	I_{DSS} mA Max.	Package
2N5638	30	4.0	10	1000	10	4.0	30	50	—	TO-92
J111	30	3.0	10	1000	—	—	35	20	—	TO-92
U1897J	30	5.0	10	—	16	—	40	30	—	TO-92
2N5653	50	—	12	1000	10	3.5	30	40	—	TO-92
J112	50	1.0	5	1000	—	—	35	5	—	TO-92
U1898J	50	2.0	7	—	16	—	40	15	—	TO-92
2N5639	60	2.0	5	1	10	4.0	30	25	—	TO-92
U1899J	80	1.0	5	—	16	—	40	8	—	TO-92
2N5640	100	0.5	3.0	1000	10	4.0	30	5.0	—	TO-92
2N5654	100	—	12	1000	10	3.5	30	15	—	TO-92
J113	100	0.5	3.0	1000	—	—	35	2	—	TO-92
BF246	—	0.6	14.5	5000	—	—	25	10	300	TO-92
BF246A	—	0.6	14.5	5000	—	—	25	30	80	TO-92
BF246B	—	0.6	14.5	5000	—	—	25	60	140	TO-92
BF247	—	0.6	14.5	5000	—	—	25	10	300	TO-92RR
BF247A	—	0.6	14.5	5000	—	—	25	30	80	TO-92RR
BF247B	—	0.6	14.5	5000	—	—	25	60	140	TO-92RR
BF247C	—	0.6	14.5	5000	—	—	25	110	250	TO-92RR

1147
Current Regulator Tolerance ±20%

Part # TCR	Forward Current I_{F1}, V_F = 25V Min.	Typ.	Max.	Peak Operating Voltage POV, I_F = 1.1 I_{F1} (max) Min.	Limiting Voltage V_L, I_F = 1.9 I_{F1} (min) Typ.	Max.	Small Signal Dynamic Impedance Z_F, V_F = 25V, f = 1kHz Min.	Typ.	Anode Cathode Capacitance CAC, V_F = 25V, f = 1MHz Max.
500	192μA	240μA	288μA	75V	0.8V	1V	5MΩ	8MΩ	2pF
501	264μA	330μA	396μA	75V	0.9V	1.1V	3MΩ	6MΩ	2pF
502	344μA	430μA	516μA	75V	1.1V	1.3V	2MΩ	4.4MΩ	2pF
503	448μA	560μA	672μA	75V	1.2V	1.4V	1.4MΩ	3.4MΩ	2pF
504	600μA	750μA	900μA	75V	1.4V	1.6V	1MΩ	2.5MΩ	2pF
505	800μA	1000μA	1200μA	75V	1.5V	1.7V	0.8MΩ	1.9MΩ	2pF
506	1120μA	1400μA	1680μA	75V	1.8V	2V	0.6MΩ	1.4MΩ	2pF
507	1440μA	1800μA	2160μA	75V	2V	2.2V	0.5MΩ	1MΩ	2pF
508	1680μA	2100μA	2520μA	75V	2V	2.3V	0.4MΩ	0.6MΩ	2pF
509	2000μA	2500μA	3000μA	75V	2.15V	2.4V	0.35MΩ	0.5MΩ	2pF
510	2400μA	3000μA	3600μA	75V	2.25V	2.5V	0.30MΩ	0.45MΩ	2pF
511	2880μA	3600μA	4320μA	75V	2.50V	2.75V	0.265MΩ	0.35MΩ	2pF
512	3440μA	4300μA	5160μA	75V	2.75V	2.95V	0.245MΩ	0.30MΩ	2pF
513	4240μA	5300μA	6360μA	75V	2.85V	3.05V	0.210MΩ	0.27MΩ	2pF

1230
General Purpose Switch — 75Ω

Metal Package

Device	$r_{DS(ON)}$ Ω Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$I_{D(OFF)}$ nA Max.	C_{iss} pF Max.	C_{rss} pF Max.	BV_{GSS} V Min.	I_{DSS} mA Min.	I_{DSS} mA Max.	Package
2N5018	75	—	10	10	45	10	30	10	—	TO-18P
TP5114	75	5	10	0.5	45	10	30	30	90	TO-18P
TP5115	100	3	6	0.5	45	10	30	15	60	TO-18P
2N5019	150	—	5	10	45	10	30	5	—	TO-18P
TP5116	150	1	4	0.5	45	10	30	5	25	TO-18P

Plastic Package

Device	$r_{DS(ON)}$ Ω Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	$I_{D(OFF)}$ nA Max.	C_{iss} pF Max.	C_{rss} pF Max.	BV_{GSS} V Min.	I_{DSS} mA Min.	I_{DSS} mA Max.	Package
P1086RR	75	—	10	10	45	10	30	10	—	TO-92RR
J174	85	5	10	1	—	—	30	20	100	TO-92
P1087RR	100	—	5	—	45	10	30	5	—	TO-92RR
J175	125	3	6	1	—	—	30	7	60	TO-92
J176	250	1	4	1	—	—	30	2	25	TO-92
J177	300	0.8	2/25	—	—	—	30	1.5	2	TO-92

1551
Monolithic Differential Amplifier — General Purpose

Metal Package

Device	V_{GS} @ 200µA µV/°C Max.	V_{GS1-2} @ 200µA mV Max.	I_G @ 200µA pA Max.	G_{OS1-2} @ 700µA µmhos Max.	g_{fs} @ 200µ mmhos Min.	g_{fs} @ 200µ mmhos Max.	$V_{GS(OFF)}$ V Min.	$V_{GS(OFF)}$ V Max.	N.F. Or en dB Max.	I_{DSS} mA Min.	I_{DSS} mA Max.	C_{iss} pF Max.	C_{rss} pF Max.	Package
2N5196	5	5	15	1	1	4	0.7	4	20nV/$\sqrt{Hz}$	0.7	7	6	2	TO-71
2N5197	10	5	15	1	1	4	0.7	4	20nV/$\sqrt{Hz}$	0.7	7	6	2	TO-71
2N5198	20	10	15	1	1	4	0.7	4	20nV/$\sqrt{Hz}$	0.7	7	6	2	TO-71
2N5199	40	15	15	1	1	4	0.7	4	20nV/$\sqrt{Hz}$	0.7	7	6	2	TO-71

1555
Monolithic Differential Amplifier — Low Noise

Metal Package

@ 200µ Device	V_{GS} @ 200µA µV/°C Max.	V_{GS1-2} 200µ mV Max.	I_G @ 700µA pA Max.	g_{OS1-2} @ 200µA µmhos Max.	g_{fs} $V_{GS(OFF)}$ mmhos Min.	g_{fs} $V_{GS(OFF)}$ mmhos Max.	N.F. Or en V Min.	N.F. Or en V Max.	I_{DSS} dB Max.	C_{iss} mA Min.	C_{iss} mA Max.	C_{rss} pF Max.	pF Max.	Package
2N5561	5	5	—	0.3	2	3	0.8	3	50nV/$\sqrt{Hz}$	1	10	15	4	TO-71
SU2652	5	3	25	0.1	1	2	—	3	—	1	10	14	3	TO-71
SU2653	5	5	25	0.1	1	2	—	3	—	1	10	14	3	TO-71
2N3921	10	5	250	—	1.5	—	—	3	2	1	10	18	6	TO-71
2N4084	10	15	250	—	1.5	—	—	3	2	1	10	18	6	TO-71
2N5562	10	10	—	0.4	2	3	0.8	3	50nV/$\sqrt{Hz}$	1	10	15	4	TO-71
SU2356	10	5	100	—	1	2	—	3.5	50nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2356A	10	5	20	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2366	10	10	100	—	1	2	—	3.5	50nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2366A	10	10	20	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2654	10	5	25	0.1	1	2	—	3	—	1	10	14	3	TO-71
SU2655	10	10	25	0.1	1	2	—	3	—	1	10	14	3	TO-71
2N3922	25	5	250	—	1.5	—	—	3	2	1	10	18	6	TO-71
2N4085	25	15	250	—	1.5	—	—	3	2	1	10	18	6	TO-71
2N5563	25	15	—	0.5	2	3	0.8	3	50nV/$\sqrt{Hz}$	1	10	15	4	TO-71
SU2367	25	10	100	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2367A	25	10	20	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2368A	25	15	20	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2368	25	15	100	—	1	2	—	3.5	50nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2656	25	15	25	0.1	1	2	—	3	—	1	10	14	3	TO-71
SU2080	35	15	500	—	1.5	—	—	4	2	1	10	18	6	TO-71
SU2369A	40	20	20	—	1	2	—	3.5	15nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2369	40	20	100	—	1	2	—	3.5	50nV/$\sqrt{Hz}$	0.5	10	16	4	TO-71
SU2081	60	15	500	—	1.5	—	—	4	2	1	10	18	6	TO-71

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Analog multiplier measures phase

Alan Rich
Analog Devices Semiconductor, Wilmington, MA

You can measure the relative phase of input lines in a 3-phase power system by using **Fig 1**'s circuit. It employs a 4-quadrant multiplier, one input of which monitors reference phase $V_R\sin\omega t$. Applying a test phase $V_T\sin(\omega t-\phi)$ to the other input and introducing an additional 90° phase shift between the inputs produces an average product voltage proportional to the sine of phase angle ϕ.

One ac input, P_1, serves as the reference phase and circuit power supply. The second ac input, P_2, is the line under test. If the test phase is 120° from the reference phase, LED_1 lights; LED_2 lights when the test phase is −120° from the reference phase. When the test phase and reference phase are the same, LED lights.

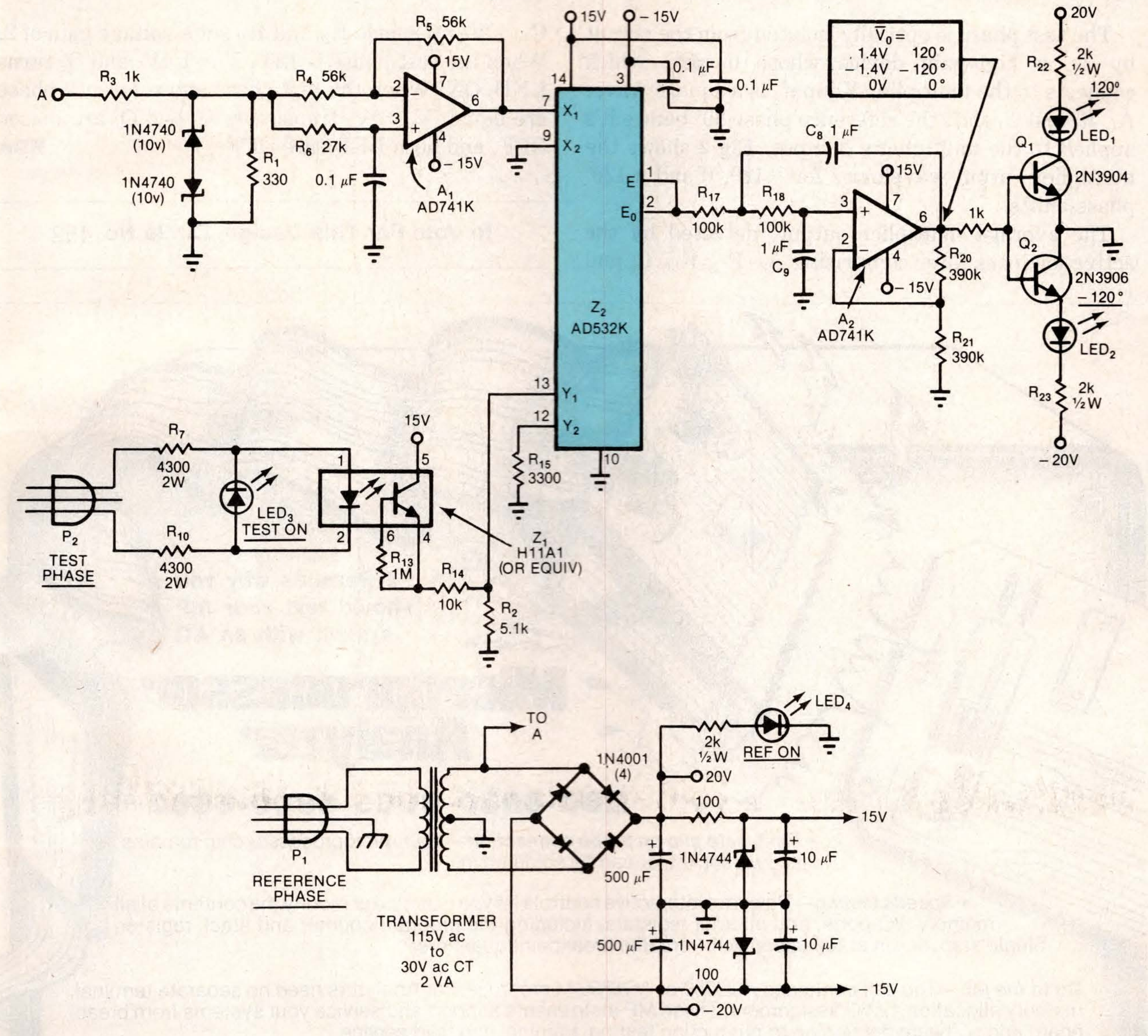

Fig 1—A 4-quadrant-multiplier-based circuit *measures the relative phase of two inputs by shifting the reference phase 90° and multiplying it by the test phase. The resulting output is an analog signal proportional to the sine of the phase angle.*

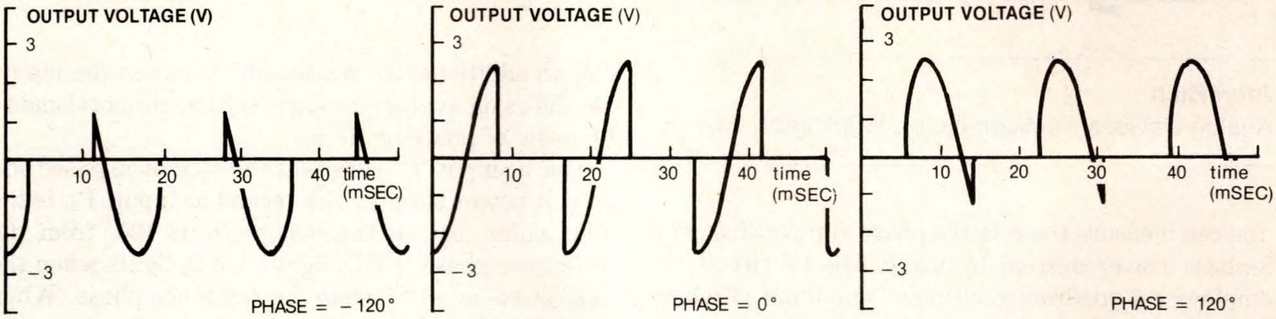

Fig 2—Multiplier output voltages for ±120° phase shifts show an average value of ±0.5V, respectively. For a phase shift of 0°, the average value is zero.

The test phase is optically isolated from the circuit by Z_1, a high-gain device whose output, which connects to the multiplier Y input, is a square wave. A_1, R_6 and C_1 shift the reference phase 90° before it's applied to the multiplier's X input. **Fig 2** shows the multiplier output waveforms for −120, 0 and +120° phase shifts.

The average multiplier output, detected by the active low-pass filter comprising A_2, R_{17}, R_{18}, C_8 and C_9, is $V_O=0.8\sin\phi$. R_{20} and R_{21} set a voltage gain of 2. When the test phase is 120°, $V_O=1.4V$, and Q_2 turns LED_2 ON. When the test phase and reference phase are equal, $V_O=0V$, transistors Q_1 and Q_2 are biased OFF, and both LEDs are OFF. **EDN**

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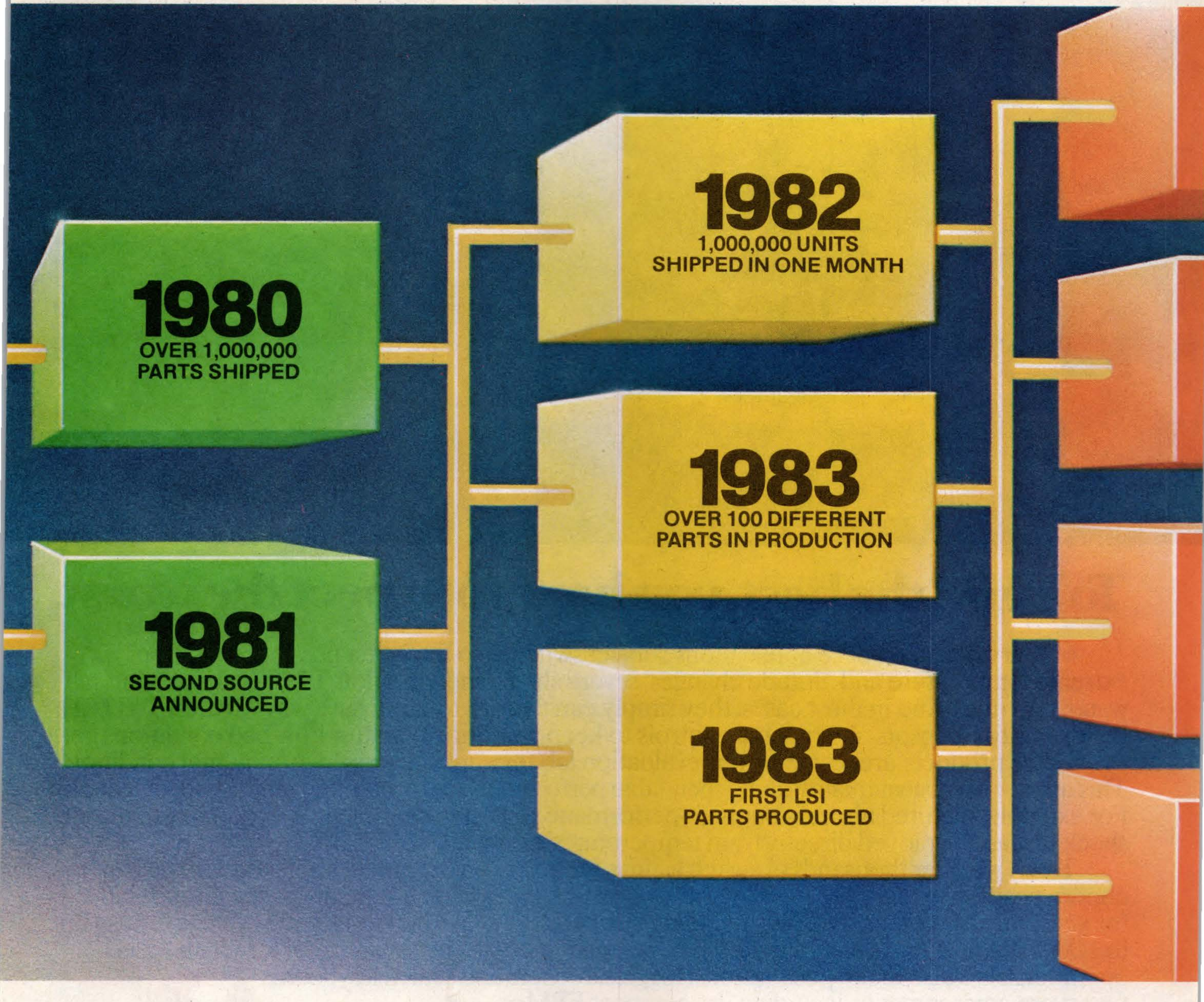

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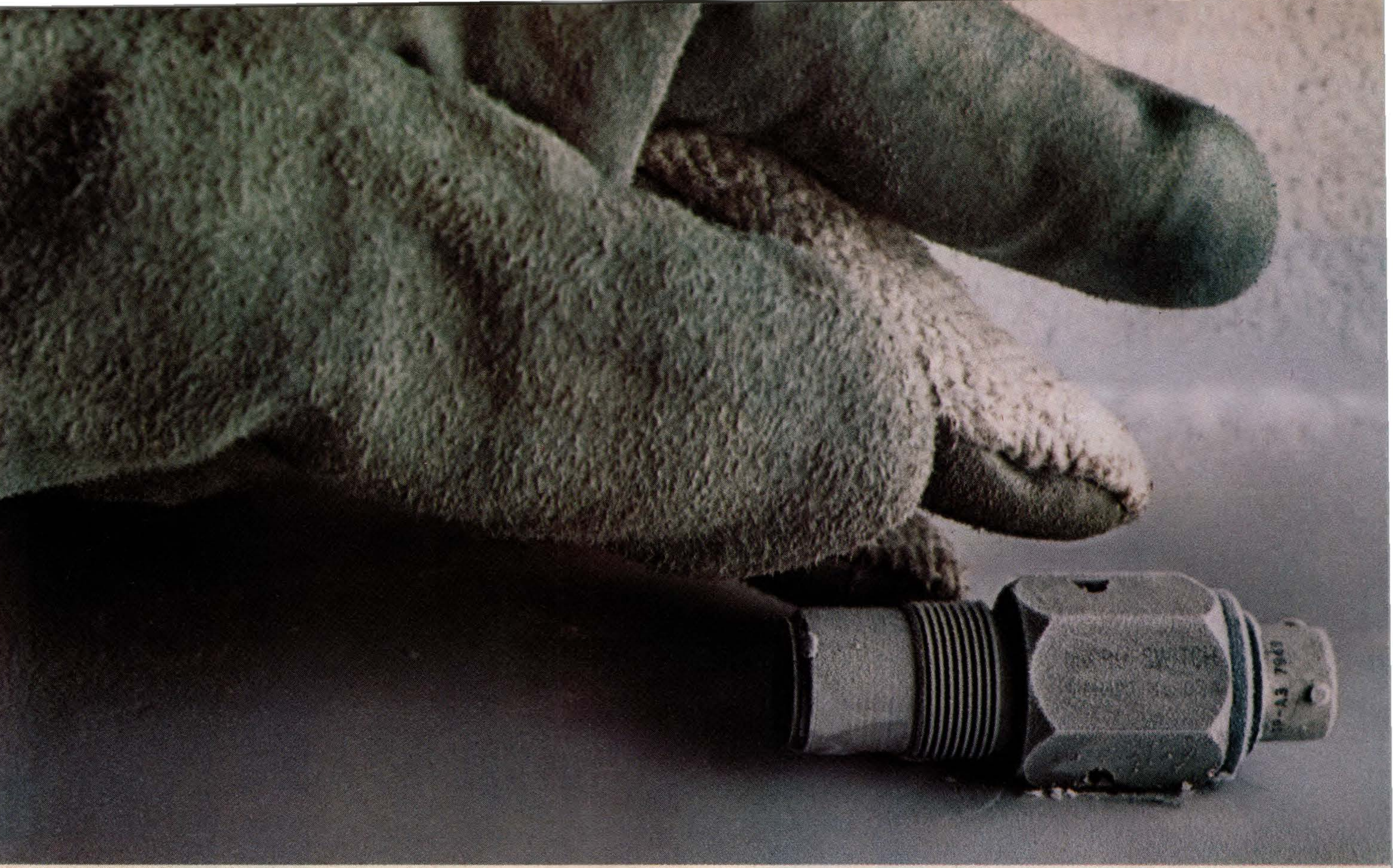

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CIRCLE NO 64

FIFO procedure prevents I/O bottleneck

Donald C Duff
Telecommunications Techniques, Gaithersburg, MD

A μC program that sends data to a slow output device such as a printer can waste a lot of time just waiting for the device to accept each output byte. By providing a first-in, first-out (FIFO) data buffer, though, the 8080/8085 routine presented here lets your program store each data byte in memory and go on to other useful tasks. A simple interrupt handler added to your program can then output a data byte each time the device is ready to receive.

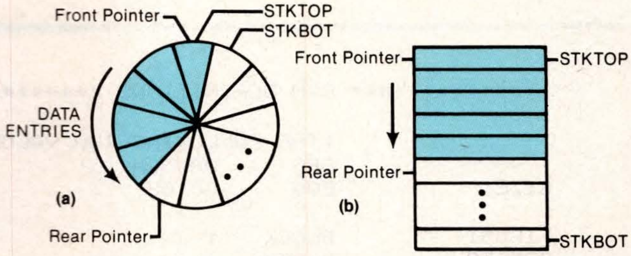

Fig 1—A circular FIFO buffer (a) *permits the removal of first-entered data entries without the need for shifting the remaining data. Two pointers mark the start and end of resident data, and parameters STKTOP and STKBOT indicate the buffer's position in memory* ***(b)***.

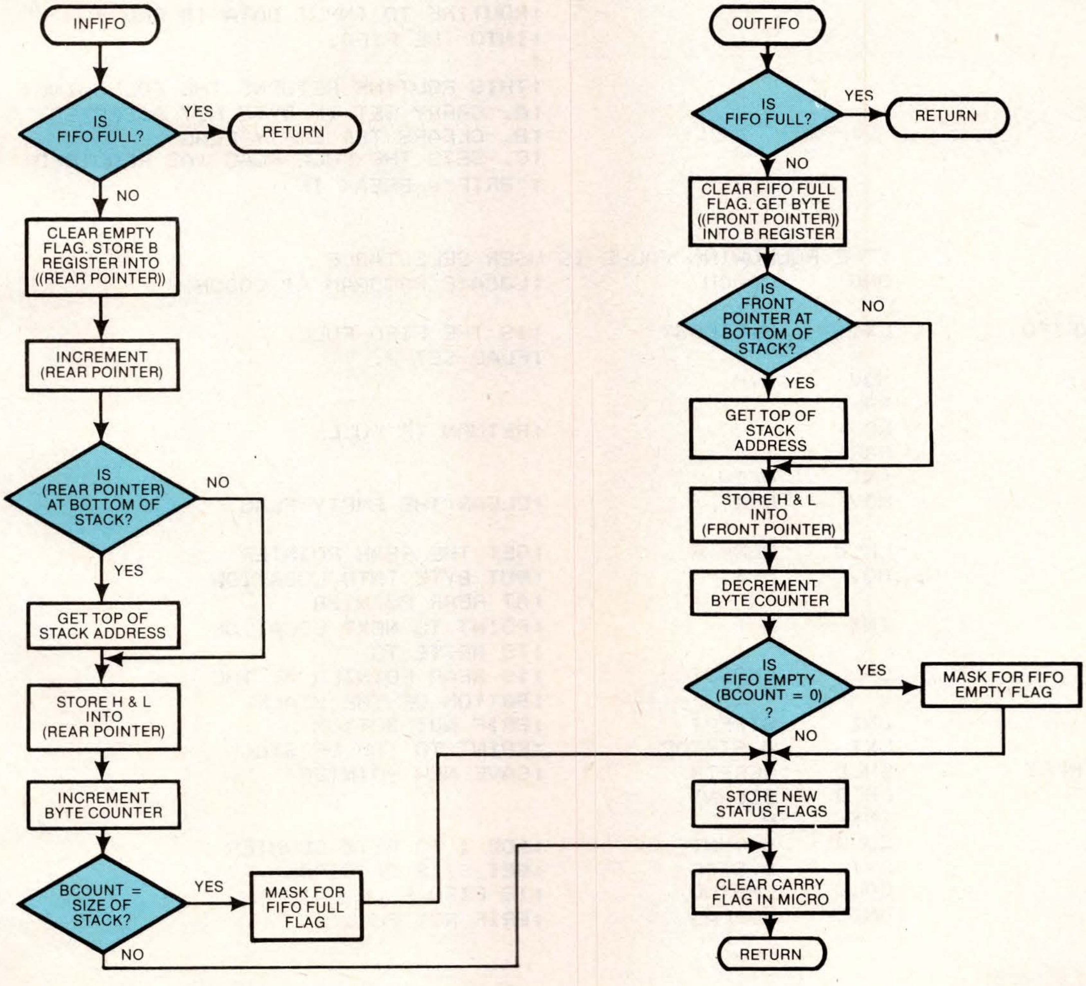

Fig 2—Routines INFIFO and OUTFIFO *add and delete buffer data. A Front pointer and a Rear pointer indicate the data's current extent in memory.*

A FIFO buffer is somewhat like a waiting line: The first data item placed in the buffer is the first out. Eventually, data at the bottom of the buffer makes its way to the top.

Just as the people in a waiting line shuffle forward, though, a straightforward implementation of a FIFO procedure requires shifting all the remaining data upward whenever any data goes from the top of the buffer to an output device. A circular FIFO buffer is an improvement on this time-consuming method.

With a circular buffer, two pointers **(Fig 1a)** eliminate the need for shifting the mass of data. A

```
;************* RAM DEFINITIONS ****************
;
              ;THE FOLLOWING TWO VALUES ARE USER SELECTABLE
              ORG     0A000H          ;LOCATE ALL RAM AT A000H AND UP
SIZE          EQU     0010H           ;LET SIZE OF STACK EQUAL 16 BYTES
;
FIFOST        BLOCK   1               ;FIFO FULL AND FIFO EMPY FLAGS
FRTPTR        BLOCK   2               ;FRONT POINTER
RERPTR        BLOCK   2               ;REAR POINTER
BCOUNT        BLOCK   2               ;BYTE COUNT IN FIFO
STKTOP        BLOCK   SIZE            ;TOP OF STACK (SIZE = SIZE OF STACK)
STKBOT        BLOCK   1               ;BOTTOM OF STACK
;
;
;NOTE: BLOCK = RESERVE BYTE(S)

                                      ;ROUTINE TO INPUT DATA (B REG.)
                                      ;INTO THE FIFO.
                                      ;
                                      ;THIS ROUTINE RETURNS THE FOLLOWING:
                                      ;A. CARRY SET IF BYTE NOT ACCEPTED
                                      ;B. CLEARS THE EMPTY FLAG
                                      ;C. SETS THE FULL FLAG (AS REQUIRED)
                                      ;"BRIF"= BREAK IF

              ;THE FOLLOWING VALUE IS USER SELECTABLE
              ORG     0000H           ;LOCATE PROGRAM AT 0000H
;
INFIFO        LXI     H,FIFOST        ;IS THE FIFO FULL
                                      ;FLAG SET ?.
              MOV     A,M
              RAL
              RC                      ;RETURN IF FULL
              RAR
              ANI     0FEH
              MOV     M,A             ;CLEAR THE EMPTY FLAG

              LHLD    RERPTR          ;GET THE REAR POINTER
              MOV     M,B             ;PUT BYTE INTO LOCATION
                                      ;AT REAR POINTER
              INX     H               ;POINT TO NEXT LOCATION
                                      ;TO WRITE TO
              CALL    CMPBOT          ;IS REAR POINTER AT THE
                                      ;BOTTOM OF THE STACK
              JNZ     STRFPT          ;BRIF NOT BOTTOM
              LXI     H,STKTOP        ;POINT TO TOP OF STACK
STRFPT        SHLD    RERPTR          ;SAVE NEW POINTER
              LHLD    BCOUNT
              INX     H
              SHLD    BCOUNT          ;ADD 1 TO BYTE COUNTER
              LXI     D,SIZE          ;GET SIZE OF STACK
              CALL    CMPTWO          ;IS FIFO FULL
              JNZ     NOFLAG          ;BRIF NOT FULL
```

Fig 3—These FIFO buffer routines, *written in 8080/8085 assembly code, keep a μP from wasting time when interfacing with slow output devices.*

```
          LDA    FIFOST       ;SET FULL FLAG
          ORI    80H
          JMP    SETFLAG      ;JMP TO CLEAR CARRY
                              ;ROUTINE TO EXTRACT DATA
                              ;FROM THE FIFO. RETURNS
                              ;DATA IN REG. B


                              ;THIS ROUTINE RETURNS THE FOLLOWING:
                              ;A. CARRY SET IF BYTE NOT VALID
                              ;B. SETS THE EMPTY FLAG
                              ;C. CLEARS THE FULL FLAG

OUTFIFO   LXI    H,FIFOST     ;IS THE FIFO EMPTY?
          MOV    A,M
          RAR
          RC                  ;RETURN IF EMPTY
          RAL
          ANI    7FH          ;CLEAR THE FULL FLAG
          MOV    M,A
          LHLD   FRTPTR       ;GET THE FRONT POINTER
          MOV    B,M          ;MOVE BYTE INTO B REG.
          INX    H            ;POINT TO NEXT LOCATION TO READ

          CALL   CMPBOT       ;IS FRONT POINTER AT BOTTOM
                              ;OF THE STACK
          JNZ    STRRPT       ;BRIF NOT AT BOTTOM
          LXI    H,STKTOP     ;GET TOP OF STACK LOCATION
STRRPT    SHLD   FRTPTR       ;SAVE NEW FRONT POINTER
          LHLD   BCOUNT       ;SUBTRACT 1 FROM BYTE COUNTER
          DCX    H
          SHLD   BCOUNT
          LXI    D,0000       ;IS BYTE COUNT = ZERO (FIFO EMPTY)
          CALL   CMPTWO
          JNZ    NOFLAG       ;BRIF NOT EMPTY
          LDA    FIFOST       ;SET THE FIFO EMPTY FLAG
          ORI    01H
SETFLAG   STA    FIFOST       ;STORE NEW STATUS FLAGS
NOFLAG    ORA    A            ;CLEAR CARRY
          RET
;
;
                              ;SUBROUTINES

                              ;ROUTINE TO COMPARE HL TO BOTTOM OR DE
                              ;RETURNS ZERO FLAG SET IF THEY COMPARE
CMPBOT    LXI    D,STKBOT     ;SET DE TO LOCATION OF
                              ;THE BOTTOM OF THE STACK
CMPTWO    MOV    A,E          ;COMPARE HL TO DE
          CMP    L
          RNZ                 ;RETURN IF THEY DO NOT COMPARE
          MOV    A,D
          CMP    H
          RET

                              ;ROUTINE TO INITILIZE THE FIFO
INTFIFO   LXI    H,0000
          SHLD   BCOUNT       ;ZERO BYTE COUNT
          LXI    H,STKTOP     ;SET FRONT AND REAR POINTERS
                              ;TO THE TOP OF THE STACK
          SHLD   FRTPTR
          SHLD   RERPTR
          MVI    A,01H
          STA    FIFOST       ;CLEAR FIFO FULL FLAG
                              ;AND SET FIFO EMPTY FLAG
          RET
```

Front pointer indicates the data item at the front of the line, and a Rear pointer indicates where the next added data item goes.

The removal of data from the front of the buffer thus moves the Front pointer around the circle, and the pointer's revised position indicates that previously used buffer space is available for storing new data. Similarly, adding data to the end of the buffer moves the Rear pointer around. The buffer's size isn't unlimited, though, so the software can't allow the Rear pointer to pass the Front pointer.

The key to the circular buffer's implementation lies in detecting when either of the pointers goes past the bottom (STKBOT) of the buffer's memory space (**Fig 1b**). The software then resets the pointer to the top of the buffer (STKTOP).

The 8080/8085 implementation of the FIFO procedure appears in **Fig 2**'s flowchart and **Fig 3**'s program listing. The program maintains a 16-bit count (BCOUNT) of the number of bytes in the buffer, and it also has a 1-byte status register, FIFOST. BCOUNT directly affects two flags in the status register: The FIFO Full flag prevents overwriting buffer data, and the FIFO Empty flag prevents reading meaningless data from the buffer.

The program consists of three routines—INFIFO, OUTFIFO and INTFIFO. To add a byte to the buffer, you call INFIFO with the data byte in register B. A call to OUTFIFO, on the other hand, removes a byte from the buffer and returns it to the calling routine in register B. INTFIFO is an initialization routine that your program must call before calling INFIFO or OUTFIFO. It sets both the Front pointer and the Rear pointer to the top of the buffer, sets BCOUNT to zero, sets the FIFO Empty flag and clears the FIFO Full flag.

If the μP's Carry flag is set on return from INFIFO, the buffer was already full and the data byte couldn't be accepted. Similarly, a set Carry flag on return from OUTFIFO indicates that the buffer was empty and the byte in register B is meaningless. You can also check the buffer's status before calling INFIFO or OUTFIFO by directly testing the FIFO Full and FIFO Empty flags. **EDN**

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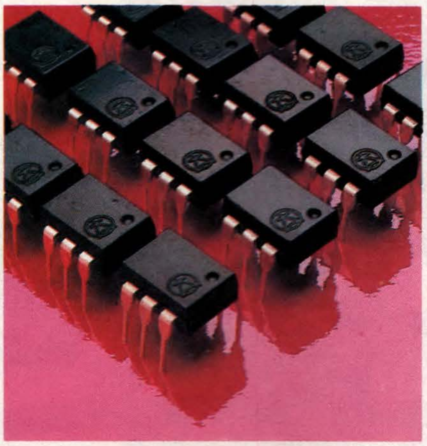

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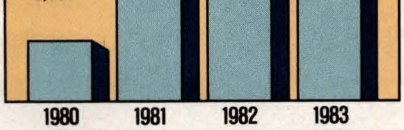

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The Hitachi 2K x 8 EEPROM Low Cost Solution To Nonvolatile Electrically Erasable Memories

The Hitachi HN48016P 2K x 8 high-density E^2PROM uses proven MNOS technology to achieve low cost with reliable nonvolatile data retention.

- Incorporates highly reliable N-channel silicon gate MNOS technology... an established technology commercially proven in demanding consumer electronic applications
- Erase and write cycle endurance of 10,000 times minimum. Ask for a copy of our reliability report
- Outstanding data retention... over 10 years at 85°C
- Famous Hitachi Quality Control, including 100% dynamic high-temperature burn-in on every unit sold
- JEDEC-approved byte-wide 24-pin DIP package... pin-for-pin compatible with industry-standard 16K bit 2716 EPROMs. Programming is 2716 compatible
- Pin-out compatible with Hitachi's 16K HM6116 2K x 8 high-speed CMOS static RAM
- Low-power dissipation — 300mW maximum
- +5V reading... +5V and +25V programming and erasing
- 350 ns maximum access time (250 ns typical)
- Can be electrically reprogrammed on board, in the field, making it ideal for all types of applications that can benefit from instant, on-the-spot data updating
- Use with microcomputers, minicomputers, and all other devices that must rely on a nonvolatile memory design to preserve data under all types of operating conditions

Best of All, It's Available NOW For Immediate Delivery at a 100 Piece Price Under $10.00

To learn more about Hitachi's HN48016P 16K E^2PROM, return coupon or call your local Hitachi Representative or distributor sales office for complete information.

YES, I am interested in receiving further information about the Hitachi HN48016P 16K E^2PROM.

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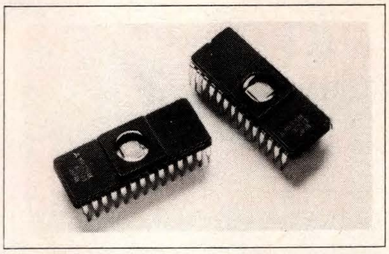
ICs & Semiconductors

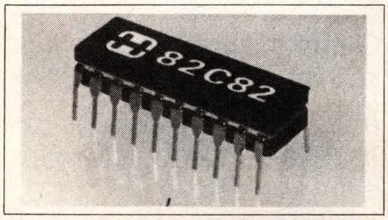


64k EPROM. M5L2764K electrically reprogrammable and ultraviolet-light-erasable memory employs n-channel double-polysilicon-gate technology in an 8k×8 organization. In Active mode, it requires 150 mA max from its 5V power supply. In Standby mode, it uses only 35 mA max. Inputs and outputs are TTL compatible in both Read and Program modes, and a 3-state output buffer facilitates interfacing. The device also furnishes two enable-control lines: Output Enable and Chip Enable. The unit comes in three versions: M5L2764K-2, with 200-nsec access time; M5L2764K, with 250-nsec access time; and M5L2764K-3, with 300-nsec access time. $24, $18 and $16.50 (100), respectively. **Mitsubishi Electronics America Inc,** 1230 Oakmead Parkway, Suite 206, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 300

HIGH-CURRENT RECTIFIERS. These low-cost epitaxial-silicon units can serve as output rectifiers and flywheel diodes in high-frequency pulse-width-modulator and switched-regulator applications. With reverse-recovery time <35 nsec, Models RUR-810, -815, -820 and -D810, -D815 and -D820 provide speeds equivalent to those of many Schottky rectifiers commonly used in switching regulator supplies. RUR-810 Series devices are single-rectifier types; the RUR-D810 family, dual-chip common-cathode units. Both families rate average forward current of 8A per chip and are spec'd for maximum forward voltage drop (V_F) of 0.89V at forward current of 8A and junction temperature of 100°C. Models -820 and -D820 can withstand maximum reverse voltage (V_{RM}) of 200V. -810 and -D810 parts carry V_{RM} ratings of 100V; -815 and -D815, −150V. RUR-810, $0.80; RUR-815, $0.85; RUR-820, $1.01; RUR-D810, $1.29; RUR-D815, $1.43; RUR-D820, $1.64. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876. Phone (201) 685-7102.

Circle No 301



BUS DRIVER. Model 82C82 octal latching bus driver is designed using its manufacturer's advanced scaled SAJI IV CMOS process, features power dissipation of 55 μW and has gated inputs that disable device inputs while data is latched. Its timing specifications equal those of the similar-grade Intel 8282 bipolar device, with propagation delay of 35 nsec guaranteed over specified operating temperature and voltage ranges and with a 300-pF load. The part comes in a 20-pin Cerdip in industrial (−40 to +85°C) and military (−55°C to +125°C) versions. ID82C82 industrial-temperature version, $7.41; MD82C82 military-temperature model, $22.24 (100). **Harris Corp Semiconductor Group,** Box 883, Melbourne, FL 32901. Phone (305) 724-7800.

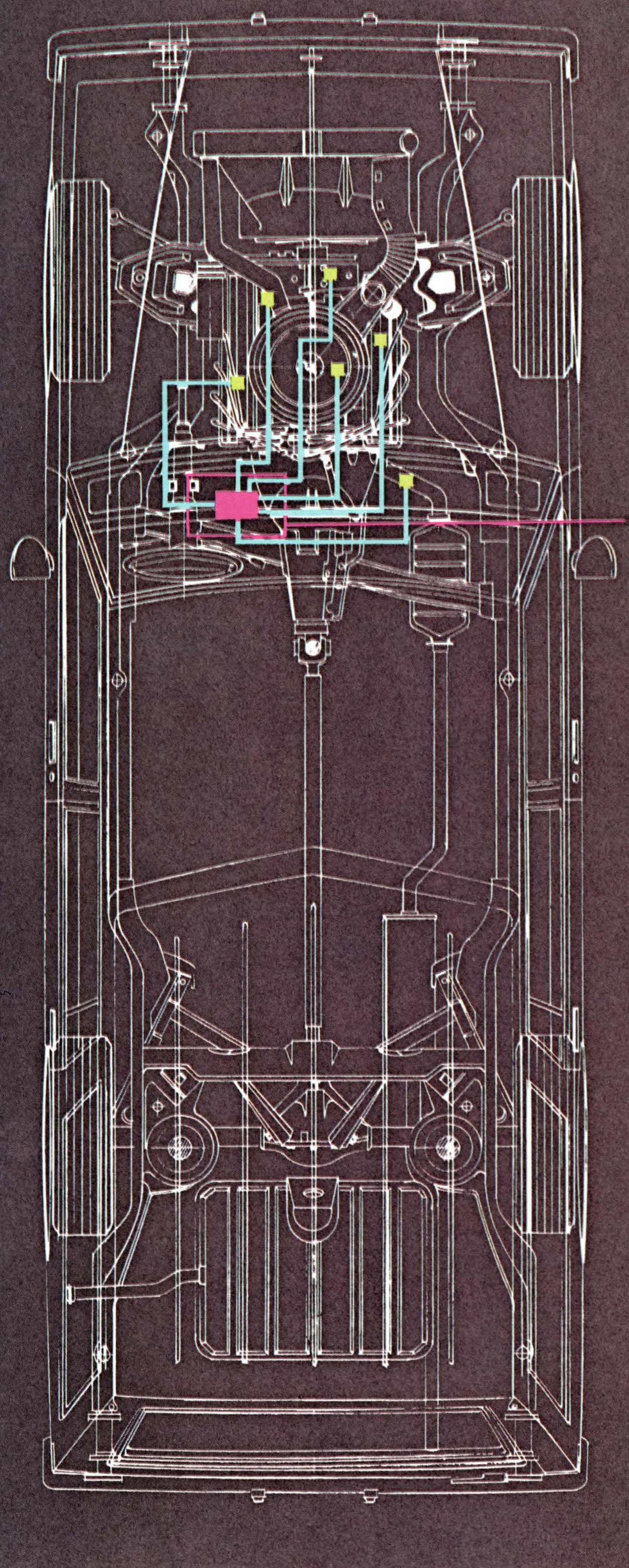
Circle No 302

Texas Instruments and GM/Delco Electronics team up to keep our air clean.

A unique automotive computer developed by Delco Electronics helps reduce exhaust emissions while still delivering good gas mileage and responsive performance.

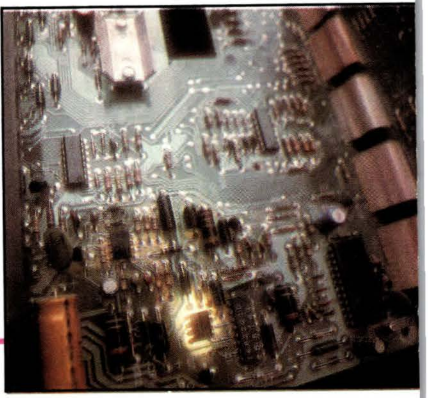
Vital to the system is an operational amplifier produced in volume by Texas Instruments. The only op amp that could meet Delco's stringent requirements.

Turn the page for more details of the TI/Delco team effort that's helping to keep our air clean. And to find out how TI's linear leadership can help you. ▶



TI's TL287 op amp is an integral part of GM's auto emission system which keeps the air/fuel mixture at the optimum level. As a result of the system, cars get lower exhaust emissions. Better gas mileage. More responsive performance.

TI cost-
cut auto



Produced in volume for the volume-oriented automotive industry

To meet environmental standards for au tomobiles, engineers of the Delco Elec- tronics division of General Motors developed a small computer that contro exhaust emissions.

For the computer to operate efficientl the signal from the exhaust sensor had t be sensed and amplified.

Here, Delco Electronics engineers hit a snag.

The problem: The source impedance from the exhaust sensor fluctuated wide How could this signal be amplified accu rately for transmission to the computer?

The solution: TI's TL287, the only operational amplifier available in volum with the necessary electrical characteris

Texas Instruments did more than sim- ply "supply" the TL287. In collaboratio with Delco Electronics engineers, we developed the procedures by which we thoroughly test each op amp before ship ment to assure dependable performance in the harsh environment of an automo tive system. And today, we continue thi cooperative testing.

Optimum air/fuel mixture helps cut pollutants

GM's system, called the Computer Com mand Control Module, keeps the air/fue mixture at the optimum level: 14.7 parts of air by weight to one part of gasoline.

The system reduces all three major forms of exhaust pollutants — nitrous oxide, carbon monoxide, and hydrocar- bons. At the same time, it is helping raise fuel economy.

effective BIFET op amps help pollutants, stretch gas mileage.

Vorld leader in BIFET op amps

he op amp Delco Electronics needed is pricated with TI's pioneering BIFET chnology.

Texas Instruments introduced the first ll family of BIFET op amps in 1976. e were the first company with volume oduction. Today, we make the indus-y's broadest line.

By 1981, 3 million cars were fitted th the TL287. How did the op amp rform? So well that, since then, Delco s ordered another 3 million units. In t, field return data from almost 5 mil-n cars on the road shows a remarkable 5-year MTBF.

TI BIFET op amps withstand harsh environments

addition to their superior electrical aracteristics, TI BIFET op amps are ell suited to harsh environments.

They perform under extremes of heat d cold. In dry or humid climates. On stems subject to jars and vibration.

Why do TI BIFET op amps perform so ell in adverse conditions? Our under-anding of plastic packaging technology d our manufacturing expertise virtually sure dependable performance.

Plastic packaging also helps make TI FET op amps cost effective. Small chip e facilitates volume production, further hancing economy.

If you need reliable op amps, in quan-y, follow Delco's lead. Come to the ader. Texas Instruments.

TI BIFET op amps: Your broadest choice of reliable solutions

he TL287 used by Delco Electronics is st one member of TI's FET input op np line. Five distinct families. Singles, als, and quads. Single and dual supply.

We produce general-purpose BIFET op nps. BIFET op amps with low noise. ow power. Very low offset voltage. FET op amps — single supply.

All members of TI's family of FET put op amps have special features that lve difficult design problems.

TI even produces a programmable low-power BIFET op amp. You can change power consumption and still maintain superior bandwidth and slew rate.

TI comparators: Only FET input, single-supply comparators available

Our TL311, TL311A, and TL311B comparators extend the operating range of the common mode input voltage to include the value of the negative V_{CC} supply. Result: no negative power supply required. The TL311 family offers fast response. Low offset. And strobe capabilities.

TI buffers: Low power, high input impedance, and economy, too

The TI TL068I and TL068C are BIFET input, unity-gain amplifiers. If you need a low cost, 3-terminal voltage follower with a combination of low power, high input impedance, fast slew rate, and wide bandwidth, one of the TI buffers will be right for your application.

TI VFD drivers: Better than the industry standard

TI produces industry standard VFD drivers, such as our new UCN4810A. But we also offer greatly improved versions: Our TL4810A, SN75512A, SN75513A, and SN75518.

Fabricated with high-voltage BIDFET* technology, TI's improved drivers feature an active totem-pole output which improves sink-current capability. Decreases interdigit blanking-time requirement. And reduces overall power consumption.

In 10-, 12-, and 32-bit (SN75518) configurations with the same or better cost-per-bit than the 10-bit industry standard.

TI peripheral drivers: The right features to meet your needs

New peripheral drivers from TI offer a combination of high output current and voltage, single-saturated output transistors, low standby power, and high-impedance PNP inputs. Available in the unique dual (SN75407 and SN75408) and industry-standard quad (SN75436, SN75437A, and SN75438) configurations.

All in reliable plastic packages.

For more information on TI linear products, contact your local TI distributor or TI sales engineer. Or fill in and mail the coupon on the next page.

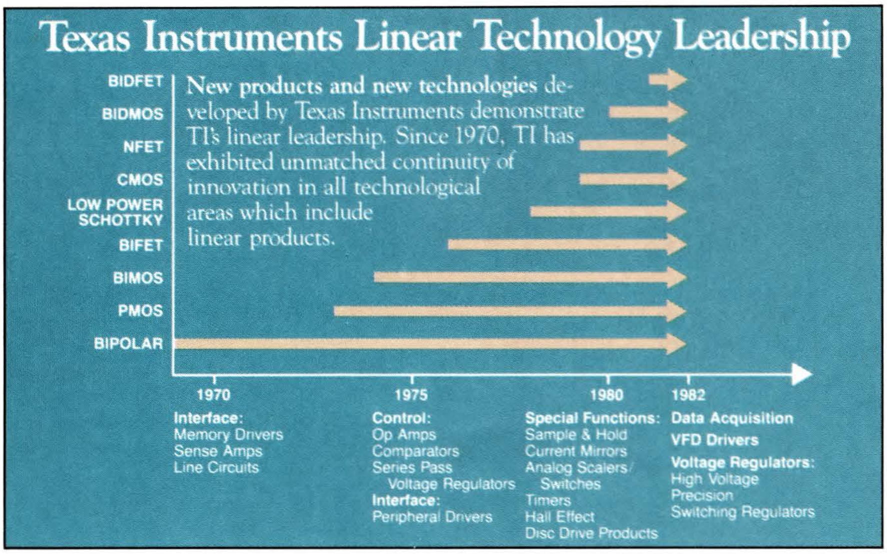
A brief history of TI BIFET technology

Year	Device(s)	Complexity	Description	Cumulative product line strength
1976	TL080 Series	Singles, duals, quads	General purpose	9
1977	More TL080s and TL070 Series	Singles, duals, quads Singles, duals, quads	General purpose Low noise	27
1978	TL060 Series	Singles, duals, quads	Low power	33
1979	More TL070s More TL060s, TL087 family	Singles Singles Singles, duals	Low noise Low power Very low input offset	43
1980	TL068 TL066 TL311 TL094	Single Single Single Quad	BIFET buffer Programmable low-power op amp NFET comparator NFET op amp (single supply)	47
1981	TL091, TL092 TL311A, TL311B TL066A, TL066B	Single, dual Singles Singles	NFET op amps NFET comparators Programmable low-power op amps	53
Total FET input line strength: 27 singles, 14 duals, 12 quads				53

TI has added 53 new members to its family of FET input linear IC functions, since 1976, almost twice as many as the nearest competitor — solid evidence of TI's linear leadership.

*Patented process of Texas Instruments.

TI linear leadership makes your system design job easier.



Texas Instruments has achieved linear leadership based on innovative technology.

Today, our linear line includes more than 500 products. This breadth of line gives you many choices of linear devices from which you can fill virtually any need.

Maintaining a sustained pace of technological innovation, we have moved from bipolar to BIFET to NFET to our latest innovative technology — BIDFET.

First in bipolar and BIFET

If the linear device you need is bipolar, chances are we have it. TI is a world leader in bipolar technology.

TI also makes the industry's broadest line of BIFET op amps and buffers. Our BIFET family includes 50 devices, almost twice as many as our nearest competitor.

In addition, we offer nine BIFETs to MIL-STD-883B, among the 147 linear devices in our military products family.

BIFET technology combines P-channel junction FET inputs with bipolar stages. On a single chip.

This combination results in circuits with performance levels never before possible. Circuits with low noise. High input impedance. Outstanding reliability.

Leading the way in NFET and BIDFET, too

Or maybe you need op amps or comparators from our NFET family. NFET op amps, pioneered by TI, are an ingenious combination of N-channel junction FET with bipolar devices — all on a single monolithic chip.

Input and output circuitry are designed to provide operation down to ground potential. As a result of this process technology, you get FET input performance combined with single-supply operation.

TI also pioneered BIDFET which combines **many** silicon technology recipes on a single chip. BIDFET allows you to get the electrical characteristics of many devices in one.

Simply stated, TI excels in virtually any technology. But maybe you just need rugged, reliable op amps, comparators, buffers, display drivers, peripheral drivers, line circuits, A-to-D converters, and voltage regulators. Once again, TI is your first choice.

Single source simplifies ordering and designing

Because of our broad line, Texas Instruments is very likely to have the linear products you need.

If you make TI the single source for your linear devices, your design job will be simplified. Ordering will be easier. You'll have access to TI applications and product engineers for any necessary design assistance. You'll handle a single set of specs for each product.

What's more, when you specify TI, you know you'll get linear products that are designed, manufactured, and tested to last.

Available in quantity from TI distributors

TI linear products are available in quantity from your local TI distributor. Call him, or your TI sales engineer.

For more information on TI's complete line of linear products, check the appropriate box in the coupon.

TEXAS INSTRUMENTS

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Dallas, Texas 75220

Please send me free literature on the following linear products:

- ☐ 1. Operational Amplifiers
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- ☐ 4. Linear Products to military specifications
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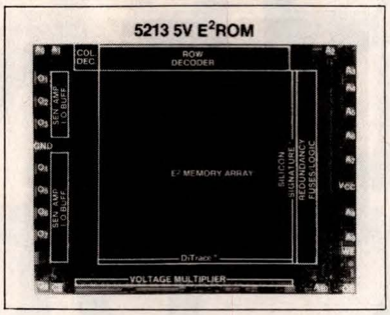
A04-068

ICs & Semiconductors

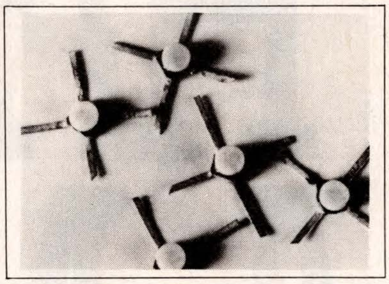


16k EEPROM. Billed as the first available 5V electrically erasable PROM, Model 5213 has 2k×8-bit organization, comes in a 24-pin DIP and can be programmed with either a TTL-level or 21V signal. Utilizing a 5V±10% power supply for read, write or erase operations, it provides an unlimited number of read cycles at 350 nsec. The device can be written or erased in <10 msec and accommodates byte-erase, byte-write and chip-erase modes. $31 (100) for 350-nsec commercial-grade version. **Seeq Technology Inc,** 1849 Fortune Dr, San Jose, CA 95131. Phone (408) 262-5041.

Circle No 303

RF/VIDEO SWITCH. The IH5341 CMOS high-speed dual monolithic switch suits high-frequency RF and video-system applications. It matches the 75Ω impedance of video communications systems and handles signal frequencies to 100 MHz with a loss of less than 3 dB. The dual spst device features OFF-isolation rejection ratio and cross-coupling isolation rejection of 60 dB min at 10 MHz; switching speeds of 150 nsec on and 80 nsec off; and guaranteed break-before-make switching. Power-supply current equals <1 mA, and power-supply range can span ±5 to ±15V. Absolute maximum ratings include supply voltage of ±17V, power dissipation of 250 mV and operating temperatures spanning −20 to +85°C (industrial) and −55 to +125°C (military). $6 (100) for the industrial component; $12 for the military version, both in TO-100 cases. **Intersil Inc,** 10710 N Tantau Ave, Cupertino, CA 95014. Phone (408) 996-5000.

Circle No 304



TRANSISTORS. These bipolar units operate over 0.1 to 6 GHz. Model AT-42035 features insertion power gain of 11.5 dB, maximum available gain of 14.5 dB, power output of +20 dBm (1-dB gain compression) with 14-dB associated gain and spot noise figure of 3 dB at 2 GHz. AT-41435-3 and -41435-5 furnish similar performance with +19-dBm output power and 9-dB associated gain at 4 GHz. The -3 version offers noise figure of 1.3 dB at 1 GHz and 3 dB at 4 GHz with associated gains of 19 dB and 10 dB, respectively. The -5 version specs insertion power gain of 18 dB at 1 GHz and 6.5 dB at 4 GHz with 3.1-dB noise figure and operates with collector current <40 mA. Typical collector efficiencies of these devices spec as high as 38%. The AT-41470 provides 16.5-dB maximum available gain at 2.0 GHz and can be qualified for military and space applications. Models AT-42035 and AT-41435-3, $6; AT-41435-5, $4.50; AT-41470; $70 (100). **Avantek Inc,** 3175 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-6710.

Circle No 305

THERE HAS BEEN A MISTAKE.

SOMEHOW, THE R6500/* HAS BECOME THE TOP 9 MICROCOMPUTERS.

One of our design engineers has gotten carried away, again. He knows Rockwell is trying not to be known as Number One in microcomputers, but he keeps coming up with winners.

His first mistake was making the R6500/1 the benchmark champ[1] among 8-bit microcomputers. We've compounded that mistake by coming up with four more R6500/*'s with more features, the same high performance and up to 56 I/O lines.

And we've continued to break the rules. Now, Rockwell International is forced to introduce four more members of the R6500/* family. Designed for use in multiple-CPU systems, the new R6500/41, /42, and /43 and R6541Q Intelligent Peripheral Controllers let you off-load control tasks from your central CPU. The necessary intelligence is downloaded into RAM through a special asynchronous host bus port, compatible with R6500, Z80, 8080, and 6800 bus structures.

Now we're stuck with a family of nine microcomputers that share the instruction set and pipeline architecture of the R6502 CPU, which continues to be the largest selling microprocessor.[2] Rockwell's exclusive software compatibility gives you the freedom to switch between single- and multiple-chip designs without starting over. For systems development, our new low-cost Design Center supports development of up to 4 concurrent processors.

Rockwell never intended to be recognized as the Top 9, the Top 5, or even the Top 1. It hasn't been our style, but you can profit from our mistake by benchmarking the R6500's in your application.

Contact your local Rockwell distributor or Sales representative, or the Electronic Devices Division, Rockwell International, at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300 Newport Beach, CA 92660.

Models	New R6541Q	New R6500/41 IPC	New R6500/42 IPC	New R6500/43 IPC	R6511Q	R6500/11	R6500/12	R6500/13	R6500/1
ROM (x8)	—	1536	1536	256	—	3072	3072	256	2048
RAM (x8)	64	64	64	64	192	192	192	192	64
I/O Lines	23	23	47	23	32	32	56	32	32
Serial Comm.	—	—	—	—	UART	UART	UART	UART	—
Counters	1x16	1x16	1x16	1x16	2x16	2x16	2x16	2x16	1x16
Expansion Bus	8K	4K	4K	4K	65K	16K	16K	65K	—
Interrupts									
External	5	4	4	5	6	6	6	6	3
Internal	1	1	1	1	4	4	4	4	1
Host	2	2	2	2	—	—	—	—	—
Standby RAM	—	—	—	—	12	12	12	12	35
Package	64-pin QUIP	40-pin DIP	64-pin QUIP	64-pin QUIP	64-pin QUIP	40-pin DIP	64-pin QUIP	64-pin QUIP	40-pin DIP

1. Benchmark test specified by Texas Instruments, including TMS7000, Z8, 8051 and R6500/1. Details provided on request.

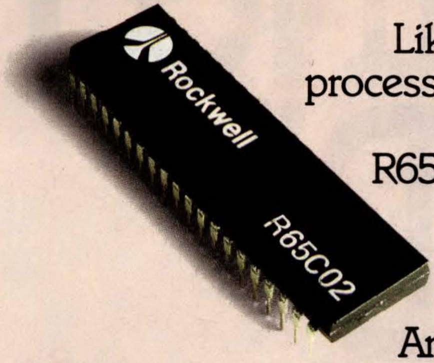
2. Source: Dataquest

Rockwell International

...where science gets down to business

CIRCLE NO 69

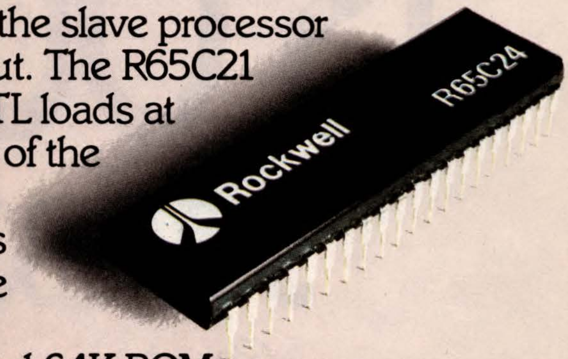
ROCKWELL'S NEW HIGH PERFORMANCE CMOS FAMILY MAY RUIN OUR REPUTATION.



Like our NMOS 8-bit family, our CMOS microprocessors seem to out-perform the competition's.

We're reluctant to admit that the 4MHz R65C02 is one of the first microprocessors, CMOS or NMOS, that can execute an instruction in half a microsecond. That its 2MHz version consumes only 40mW — 1/20 the power of the NMOS version. And that it is pin-compatible with the R6502. We've also added 12 new instructions to the R65C02 set.

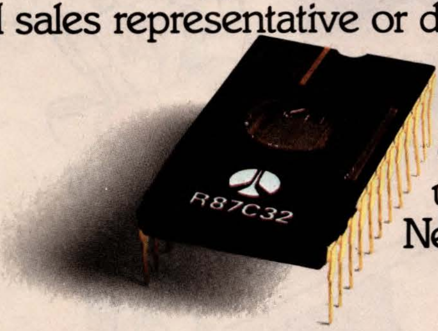
As long as we're clearing our conscience, let's also admit that the R65C02 is only one of our new CMOS designs. There's also the R65C102, a microprocessor with on-chip oscillator, and the slave processor R65C112, which accepts an external clock input. The R65C21 Peripheral Interface Adaptor that drives two TTL loads at once and the R65C24, with all the capabilities of the R65C21, plus a 16-bit counter/timer with latch.



There's also the R65C51 Asynchronous Communications Interface Adaptor. And these new CMOS RAMs and ROMs to choose from: 16K Static RAM, 32K EPROM, 64K EPROM, and 64K ROM.

And Rockwell supports system development for all Rockwell CMOS and NMOS microprocessors through SYSTEM 65 and the new Rockwell Design Center (RDC).

We can't blame you for expecting less of us. For years, we've been trying hard <u>not</u> to be recognized as Number One. But you can profit from our slip-up by trying these new CMOS parts in your application. We'll apologize in advance for providing you with higher performance and lower power consumption. For information, just contact your nearest Rockwell sales representative or distributor or the Electronic Devices Division, Rockwell International, at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, CA 92660.



Rockwell International

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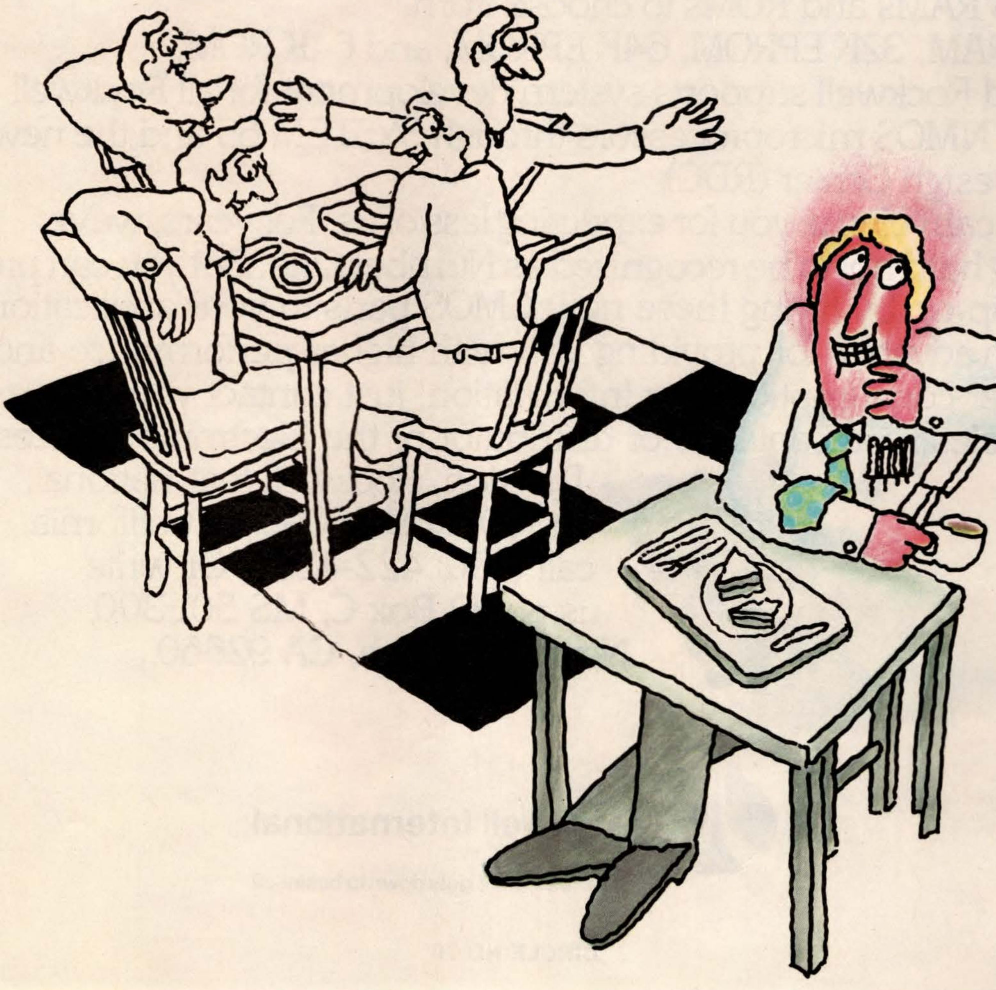
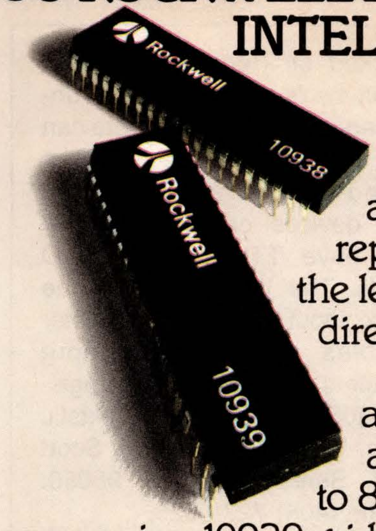
CIRCLE NO 70

"FIRST THINGS SECOND" IS OUR RULE.

SOMEBODY BROKE IT.



SO ROCKWELL HAS TO INTRODUCE FIVE NEW INTELLIGENT DISPLAY CONTROLLERS.



Our rule was already broken when we came up with the 10937, the first single-chip controller for alphanumeric displays. Now the offense has been repeated not once, but five times, to give Rockwell the leading family of intelligent controllers that directly drive VF displays of up to 60 volts.

Our new 10938, 10941, 10942, and 10943 anode drivers simplify your design job for all sizes of alphanumeric displays, from 8 character segmented to 80 character 5x12 dot matrix. All four, and the companion 10939 grid driver, accept either serial or parallel I/O. Because all of these devices have built-in intelligence, they lower your hardware costs by as much as 30¢ per character. If your product has an 80 character display, our controllers save you $24.

Besides eliminating TTL parts, Rockwell's intelligent display drivers reduce the load on your CPU by 90%, because they handle the complete display refresh function.

It's bad enough having these advanced parts for VF displays, but it doesn't stop there. All 6 work with any host processor with just 2 I/O pins through a serial interface.

We've been reluctant to talk about our leadership in display controllers. On the other hand, our distributors are loaded up with them and will be more than happy to talk about filling your order today. Check the chart to get an idea of the best combination for your application, then contact your nearest Rockwell distributor. Or the Electronic Devices Division, Rockwell International, at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, CA 92660.

GUIDE TO CHOOSING ROCKWELL DISPLAY CONTROLLERS

Display Type			
Characters	Segments/ Matrix	Anode Drivers	10939 Grid Driver
8	14-18	A single 10937 device provides anode and grid drivers for these display types.	
10	14-18		
16	14-18		
20	14-16	1 (10941)*	1
32	14-16	1 (10941)*	2
40	14-16	1 (10941)*	2
20	5x7	1 (10938)	1
32	5x7	1 (10938)	2
40	5x7	1 (10938)	2
40	5x12	1 each (10942 & 43)	2
80	5x7	1 (10938)	4
80	5x12	1 each (10942 & 43)	4

*Also controls bar graph function.

Rockwell International

...where science gets down to business

CIRCLE NO 71

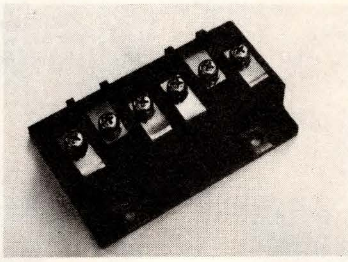
PARALLEL MULTIPLIERS. 16×16 NMOS parallel-array units, WTL2516 and WTL2517 consume less than one-fourth the power of bipolar devices and spec 200-nsec typ multiply time. Pin-for-pin functional equivalents to bipolar units such as the TRW MPY16HJ and AMD 29516/

29517, they feature I/O latches that can be operated in either Clocked or Transparent mode. 16-bit two's-complement or unsigned-magnitude input data can be accommodated, as can mixed-data-format operation. The devices operate from 5V and have TTL-compatible I/O levels. The WTL2517 has one clock input and three register enables for the two input registers and one output register. $65 (100) in 64-pin plastic DIPs. **Weitek Corp,** 3255 Scott Blvd, Santa Clara, CA 95050. Phone (408) 727-6625.

Circle No 306

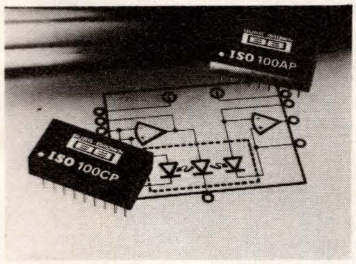
GaAs FETs. Three high-gain, low-noise units suit communications/radar and electronic-defense applications in the 6- to 18-GHz range. In unpackaged chip form, the AT-10600 features 1.5-dB noise figure and 12-dB associated gain at 6 GHz; 1.8-dB NF and 9-dB gain at 12 GHz; and 2.8-dB NF with 6-dB associated gain at 18 GHz. In a hermetic metal/ceramic 50-mil stripline package, the AT-10650-1 furnishes identical performance through 12 GHz; the AT-10650-3, a lower cost version also in the 50-mil package, provides 1.9-dB NF and 11-dB associated gain at 6 GHz; 2.3 dB and 8 dB at 12 GHz. All versions produce 17-dBm output power (at 1-dB gain compression) at 12 GHz. The GaAs FET chip used in all three transistors incorporates thick gold-plated metallization combined with a 0.5-μm gate length for small chip size, low parasitic reactance and impedance levels that are easy to match throughout its operating frequency range. AT-10600, $50; AT-10650-1, $105; AT-10650-3, $63 (100). **Avantek Inc,** 3175 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-6710.

Circle No 307



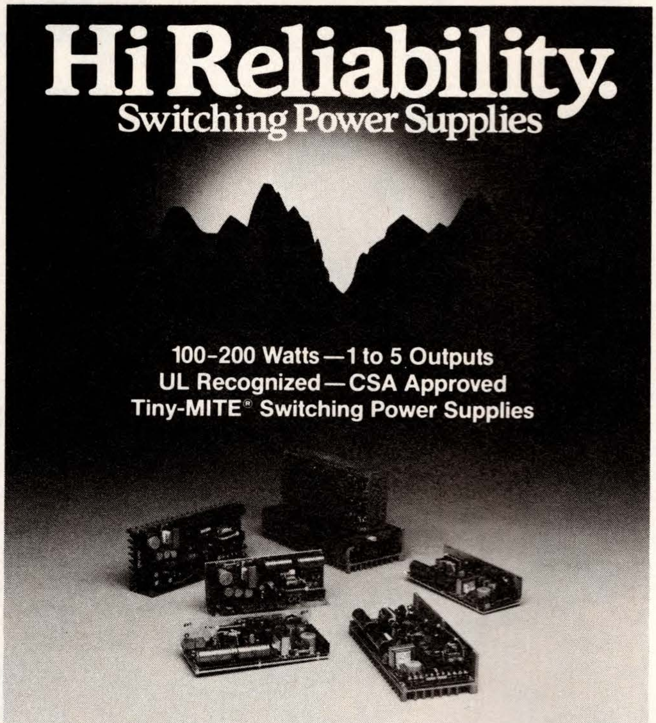
POWER MODULE. For PWM applications, the Fuji Electric 1000V 50A EV1235 switching power module contains two complete Darlingtons, internally isolated from the mounting base as well as from each other. For snubberless circuit design, the unit provides fast-recovery discrete antiparallel diodes, a square RBSOA curve and fast switching speeds, permitting PWM operation over 1 to 5 kHz. The Darlingtons are triple-diffused planar glass-passivated types, assembled as a hybrid with planar diodes. $74.38. **Collmer Semiconductor Inc,** 14368 Proton Rd, Dallas, TX 75234. Phone (800) 527-0251.

Circle No 308

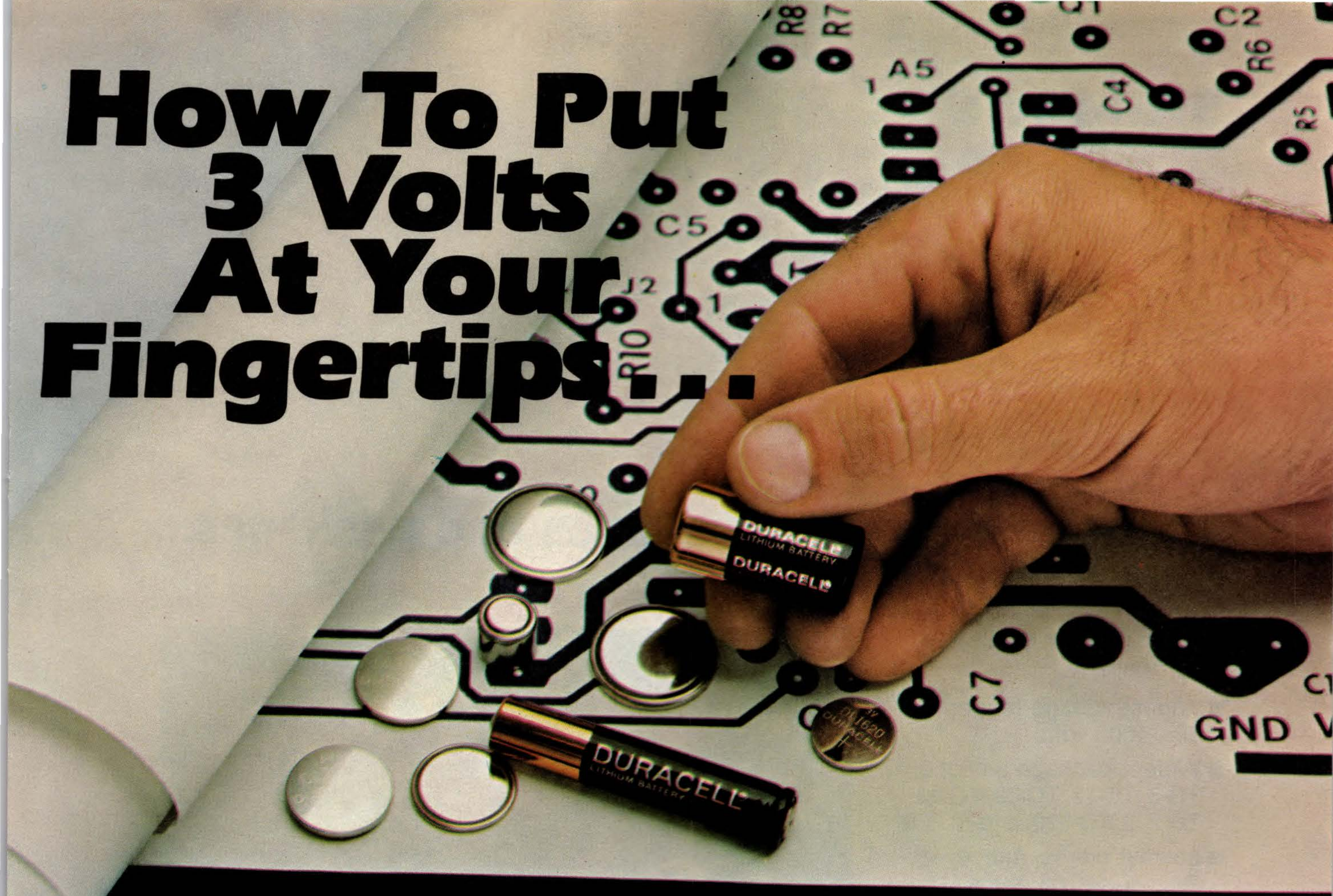


ISOLATION AMP. A low-drift, wide-bandwidth, optically coupled unit, Model ISO100 achieves a voltage-drift-vs-temperature spec six times lower at G=100 than that of its predecessors. It provides optical feedforward for isolation and optical negative feedback to linearize the transfer function and protect the gain from the effects of LED aging. Three grades are available, with maximum nonlinearity ranging from 0.4 to 0.07%, input offset voltage of 500 to 200 μV max and input offset voltage drift of 5 to 2 μV/°C max. Continuous isolation rating equals 750V between input and output terminals and is 100% tested at 2500V. Input-to-output isolation resistance specs at $10^{12}\Omega$; bandwidth, at 60 kHz. The amplifier stage furnishes 10-nA max offset current and 0.05-nA/°C max offset-current drift. $25 to $33.60. **Burr-Brown,** Analog Products Div, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111.

Circle No 309



How To Put 3 Volts At Your Fingertips...



Lithium Power... Three Volts in Less Space

Designing 3-Volt electronic packages has taken on new dimensions!

DURACELL® Lithium Batteries now afford designers the luxury of replacing two, or even three less efficient 1.5-Volt regular zinc-carbon batteries, or 1.25-Volt nickel-cadmium power sources... while gaining electrical performance.

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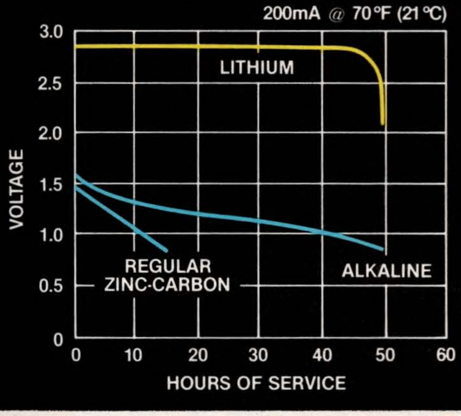
New Designs Demand New Power Sources

Today's sophisticated electronic designs require the constant power and voltage available from DURACELL® Lithium Batteries. The stable and predictable voltage output characteristic of DURACELL® Lithium Batteries make them ideal power sources for first, second or third generation products designed for increased performance and reliability.



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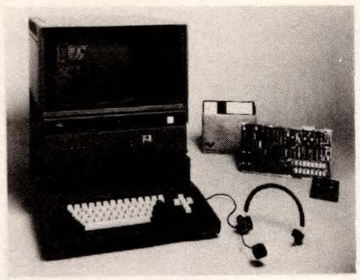


SPEECH-TRANSACTION SYSTEM. iSBC 570 Speech Transaction Development Set allows you to define a vocabulary using the iSBC 576 speech-transaction board and test the words to see that errors are minimized and recognitions occur with high rates of repeatability and accuracy. The iSBC 576 can then be combined with other iSBC boards to implement a complete speech-recognition system. Also available is the iSBC 577 Speech Transaction Chip Set, which provides the 576 board's speech-recognition function. The iSBC 570 system comprises the 576 board, a floppy disk with an application example and speech-transaction-generator software, a microphone and a new front panel for the manufacturer's Intellec development system. The board plugs into the Intellec system's chassis. The iSBC 576 provides two 2920/21 single-chip analog signal processors, an 8048 single-chip microcontroller, four 27128 (16k×8) EPROMs and an 8086 16-bit μC. iSBC 570 development set, $4900; iSBC 576 board, $2900; iSBC 577 speech-chip set, $600 (500). **Intel Corp,** 2625 Walsh Ave, Santa Clara, CA 95051. Phone (408) 987-4928.

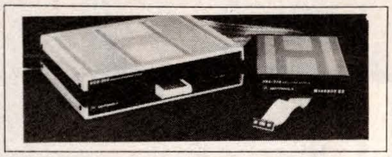
Circle No 322

SCOPE MEMORY. Model VK12-2 converts any analog oscilloscope into a digital-storage scope. Its analog-data-input unit digitizes and stores 200 bytes max of memory with 8-bit resolution, and the 2-MHz clock rate permits accurate reconstruction of analog signals to 300 kHz. An output is provided for X-Y or strip-chart recorders. Other features include trigger circuit with pretrigger feature, switch-selectable input-range sensitivity, switch-selectable timebase and memory scroll. A bit-parallel, word-serial data bus or an optional IEEE-488 bus is also available. $1495. **Soltec Corp,** 11684 Pendleton St, Sun Valley, CA 91352. Phone (800) 423-2344; in CA, (213) 767-0044. TLX 674188.

Circle No 323

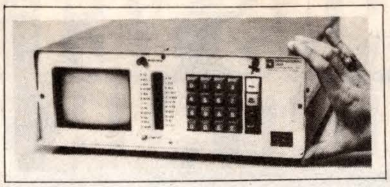
CHART RECORDERS. These X-Y units with DIN A4 8½×11-in. format feature pen speeds of 1300 mm/sec in the Y axis and 900 mm/sec in the X axis, plus dynamic response of 5 Hz. Model 6415 has 18 input ranges from 50 μV/cm to 20V/cm. Model 6414 provides nine input ranges from 2 mV/cm to 1V/cm. Both have timebases of 0.5 to 10 sec/cm. Other key specs include 1-MΩ input impedance, 0.25% accuracy, and <1% overshoot. The units also feature electrostatic paper holddown and remote control of pen lift, timebase reset and restart. From $1795. Delivery, stock to 45 days ARO. **Soltec Corp,** 11684 Pendleton St, Sun Valley, CA 91352. Phone (800) 423-2344.

Circle No 324



EMULATOR/ANALYZER. Used with its manufacturer's Exorset, Exormacs or Exorciser software-development system, HDS-200 provides a complete hardware/software-development system for the firm's M6804/M6805/M146805 families of μC chips. Comprising a control station plus a separate emulator module with an internal μC and memory capacity to match that of the chip to be emulated, the system serves as a functional substitute for the selected CPU in the target system. It provides real-time emulation, 16 programmed breakpoints, a line-by-line assembler/disassembler, program-trace commands, Help commands, memory-map display, stored macro commands and Transparent-mode operation. The HDS-200 control station contains an internal power supply, logic circuits, clock and an MC6809 that runs the monitor, controls the ports and interfaces with the emulators. Two RS-232C communication ports are included. M68HDS201 hardware-development station, $1950; emulator modules, $2000. **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. Phone (602) 244-5768.

Circle No 325



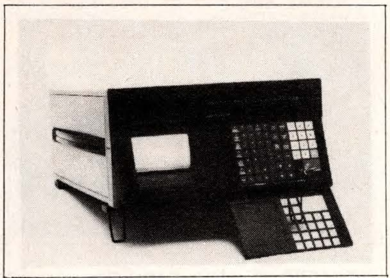
DATACOMM TESTER. Monitoring and interactively communicating with data appearing at the RS-232 interface, the μP-based Hawk 4010 locates and isolates hardware and software problems by simultaneously displaying both transmit and receive data. It can be programmed to trap and store 4096 characters and recall this data for detailed visual analysis on a 5-in. CRT. The unit operates with synchronous data rates to 19.2k bps in half- and full-duplex modes. Asynchronous operation is provided by internally generated clock speeds of 50 to 19.2k bps. Standard protocols include Bisync, SLDC (NRZ, NRZI), HDLC, X.25, ADCCP, ASCII, Baudot, EBCD, EBCDIC, Hex, IPARS, Octal, Selectric and Transcode. $4995. Delivery, 60 days ARO. **International Data Sciences Inc,** 7 Wellington Rd, Lincoln, RI 02865. Phone (401) 333-6200. TWX 710-384-1911.

Circle No 326

OSCILLOSCOPE. Featuring peak-to-peak automatic triggering and automatic focus, the 60-MHz 6.9×11×14.6-in. Model 5060 provides delay sweep, delay line, alternate sweep, a third-channel signal and a vertical signal output on the back of the unit. Sensitivity specs at 1 mV with 5× magnification. A sync separator comes standard. Other features include variable hold-off for precise adjustment of trigger hold-off time, autotriggering and peak-to-peak autotriggering. A built-in delay line permits accurate leading-edge measurements. $1100. **Kikusui International Corp,** 17819 S Figueroa St, Gardena, CA 90248. Phone (213) 515-6432.

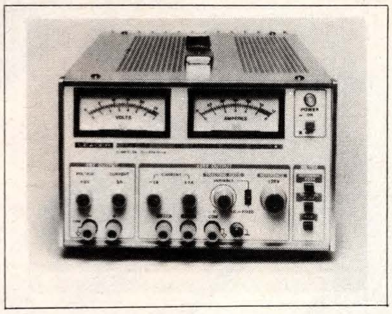
Circle No 327

Instrumentation & Power Sources



DATA LOGGER. You can expand the programmable Model 2280A from a 20-channel to a 1500-channel system with analog/digital inputs and control outputs housed in 15 remote extender chassis located as far as 1 km from the mainframe unit. Each A/D-conversion card in the system can operate to 20 readings/sec and support as many as 100 channels. Because each system can support multiple ADCs, the maximum system can be configured to operate at 100 readings/sec. The basic 2280A furnishes a library of 11 thermocouple linearizations, three RTD linearizations and four alarm limits per channel. Standard math functions include addition, subtraction, multiplication, division and parentheticals. Manipulations such as group average, time average, point difference, deviation from group average and rate of change are provided with the standard math package (advanced-math option also available). Scan-group programming affords definition of as many as 10 groups, plus group-priority management. The unit also provides a 40-column thermal printer, 40-character alphanumeric display, 12V dc operation, 32k of RAM for storing user programs and optional 500k-byte tape drive. Basic system, $7395; mainframe, $5895. **John Fluke Mfg Co Inc,** Box C9090, Everett, WA 98206. Phone (206) 342-6300. TLX 152662.

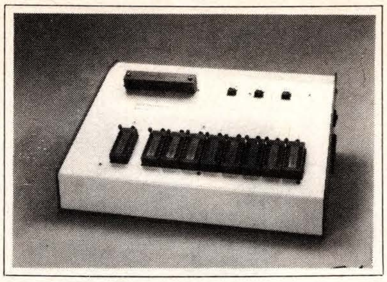
Circle No 328



POWER SUPPLIES. LPS-151 and -152 triple-output dc power supplies have metered output voltages adjustable over 0 to 6V, 0 to 25V and 0 to −25V dc. All outputs come with independent adjustable current limiting and an automatic-recovery feature that allows output voltage to return to normal when a short or overload condition is removed. Model LPS-151's output specs at 2.5A max (0 to 6V) and 0.5A max (±25V). Model LPS-152's output current measures 5.0A max (0 to 6V) and 1.0A max (±25V). Both units feature a tracking output mode that permits an adjustable ratio of positive versus negative voltage between the 25V outputs. Ripple specs at <3 mV p-p. LPS-151, $395; LPS-152, $495. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104 or (516) 231-6900. TWX 510-221-2133.

Circle No 329

EPROM COPIER. Model 8218 utilizes inexpensive personality plugs to permit copying of most widely used EPROMs and EEPROMs and automatically checks for blank copies. Non-blank EEPROMs can be erased by depressing the Program switch a second time. Sockets are cold except during active



operations to provide device protection during insertion and removal. The master socket is fully buffered, and programming is inhibited if a faulty master is detected. Blank check of the copies is performed at low V_{CC}; the post-program verify pass at high V_{CC}. Incorrect-insertion, overvoltage and overcurrent conditions are automatically detected. $1495; personality plugs, typically $25. **SMR Electronics Inc,** Box 275, Sharon, MA 02067. Phone (617) 784-2918.

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(Actual Size)

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CIRCLE NO 109

COMPONENT TESTER. Model 201 programmable curve analyzer tests transistors, Darlingtons, SCRs, triacs, optocouplers, LEDs, zeners, diodes, diacs, FETs, regulators and other discrete components. Measuring leakage currents, breakdown voltage, conducting voltages, component gains, gate-triggering parameters and holding parameters, it includes built-in test modules for parameters that can be combined to construct desired test procedures. Testing can occur in Go/No-Go mode to preset limits, or can measure parameter values. Measured data can be logged as a permanent record, including maximum and minimum limits by device type. The benchtop modular system provides an automatic programmable curve analyzer, HP-85 computer with 32k of RAM and a miniterminal with display and entry keyboard. **CIS Testronics,** 1324 Millwood Rd, McKinney, TX 75069. Phone (214) 542-5682.

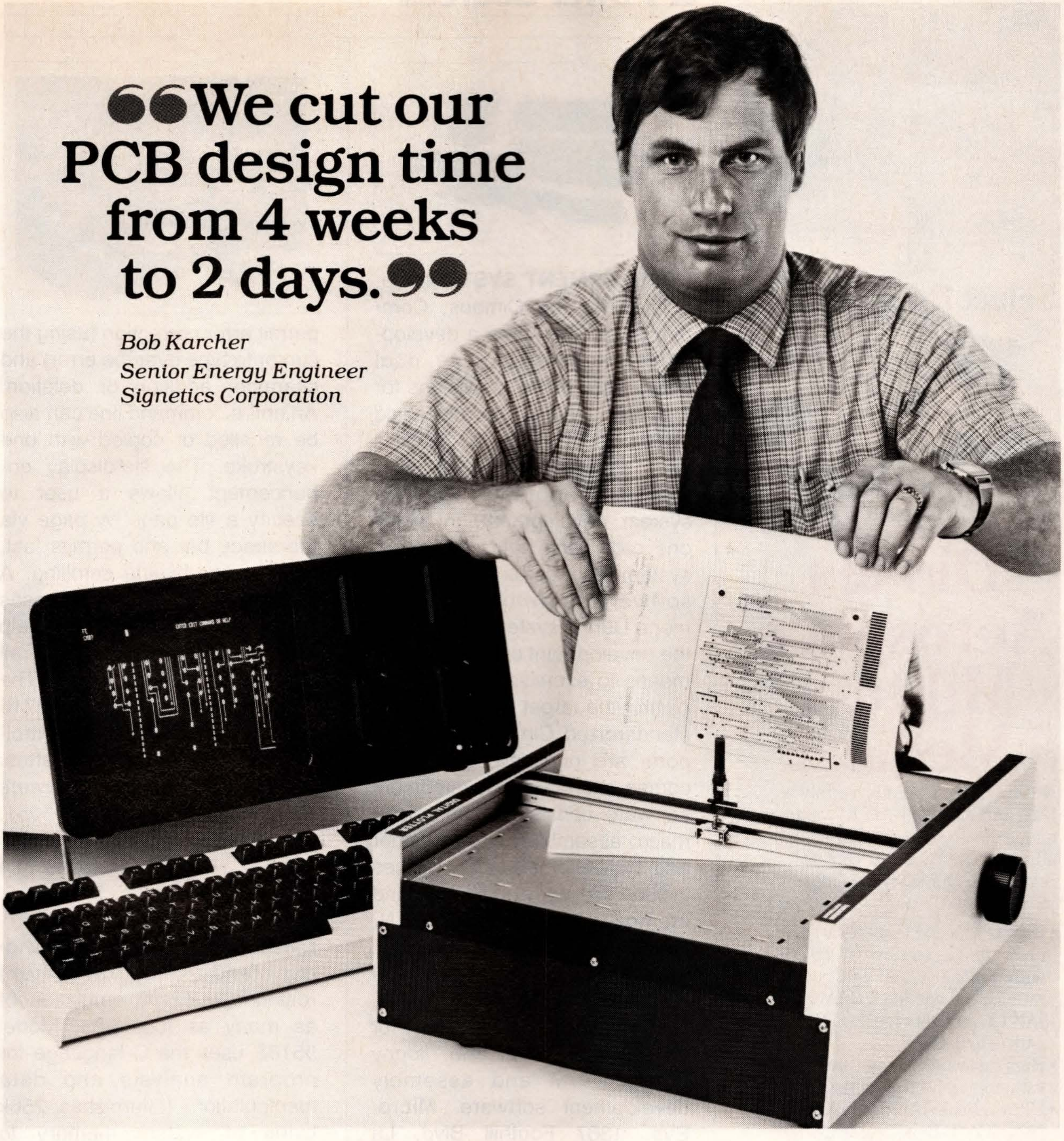
Circle No 331

DIGITAL THERMOMETERS. Capable of using two thermocouple types from a choice of 11, Models AN6501, 6502 and 6503 display direct temperature readings with 0.1°C resolution and ±0.2°C conformity to NBS-published tables. The μP-based units read temperature from −200 to +1820°C and indicate functions on a 5-digit LCD. Each supplies reference-junction compensation for Types J, K, T, E, R, S, B, N, Platinel II, J-DIN and T-DIN thermocouples and can also measure uncompensated signals from −9.988 to +99.998 mV. Model AN6503 is a digital thermometer and simulator with selectable Celsius/Fahrenheit functions, peak-temperature measurement and display-freeze capability. Model AN6501 is a dedicated digital thermometer. All units operate from a 1000-charge/discharge-cycle NiCd battery pack. Model AN6503, $695. **Analogic Corp,** 14 Electronics Ave, Danvers, MA 01923. Phone (617) 777-4500. TWX 710-348-0425.

Circle No 332

“We cut our PCB design time from 4 weeks to 2 days.”

Bob Karcher
Senior Energy Engineer
Signetics Corporation



Bob further reports, “Who would believe an investment of $1450 could deliver better, faster results than a CAD unit costing 10 times as much?

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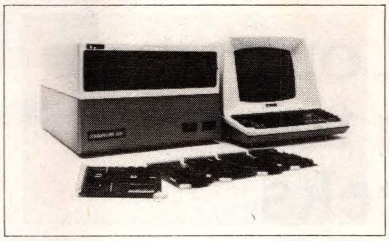
CIRCLE NO 112

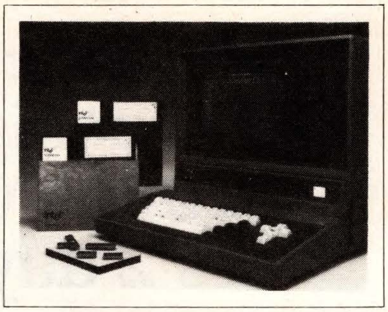
Instrumentation & Power Sources



DEVELOPMENT SYSTEM. Optimized for the Cimbus, Commander/800 features a development-software package, dual floppy-disk drives, provisions for a printer and CRT terminal and front access to all 16 Cimbus card slots. it uses the bus-exerciser approach for μC-system development, in which one card cage holds the target system and cards that control software/hardware development. During system debugging, the development cards provide a means to exercise, monitor and control the target system via the standardized Cimbus. RS-232C ports are provided, and CP/M comes standard. Development software consists of an editor, macro assembler, linking loader and symbolic debugger. Utilities include file copy, disk test and memory test. FORTRAN, BASIC, Pascal, C and FORTH are optional. $9950 for NSC800 processor, 32k of CMOS RAM, CRT terminal, RS-232C port for serial printer, dual 8-in. floppy disks, CP/M and assembly development software. **Micro/Sys,** 1367 Foothill Blvd, La Canada, CA 91011. Phone (213) 790-7267.

Circle No 333

DEVELOPMENT - SYSTEM ADD-ONS. For Intellec Series II and III μP development systems, iMDX 511 human-interface enhancements facilitate file viewing, speed up command-line editing and add a help facility. Command-line editing and recall



permit error correction (using the cursor to type over the error) and character addition or deletion. An entire command line can also be recalled or copied with one keystroke. The file-display enhancement allows a user to specify a file page by page via the space bar and permits fast, slow or line-by-line scrolling. A function-key capability accesses 41 system commands; the help facility displays a menu of all available function keys. The upgrade kit consists of four 2716 EPROMs, a 8741 microcontroller and two flexible diskettes. $375. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-9484.

Circle No 334

EMULATION SYSTEM. Providing stand-alone, transparent real-time in-circuit emulation of as many as four μPs, Model 9516S uses the C language for program analysis and data manipulation. It furnishes 256k bytes of system memory to implement features such as programmable soft keys, symbol handling and access to local mass storage for user programs and files. Communications software supports serial communication to any host with special support for PDP-11 and VAX computers. $13,470. **Gould Inc Instruments Div,** 4600 Old Ironsides Dr, Santa Clara, CA 95050. Phone (408) 988-6800.

Circle No 335

Brown Disc introduces hard disc capability with the convenience and low cost of a floppy.

Only Brown Disc offers processing technologies normally associated with hard disc manufacturing: An exclusive spin coating technique produces a thinner coating with high bit integrity for ultra-hi densities. A special overcoat and primer layer are used to increase adhesion, disc life and head life. Plus individual stress relieving improves substrate stability.

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UHR-I	60 μ in.	300 oersted	10,000 BPI	3.2 megabyte
UHR-II	45 μ in.	600 oersted	10,000-18,000 BPI	5.0 megabyte

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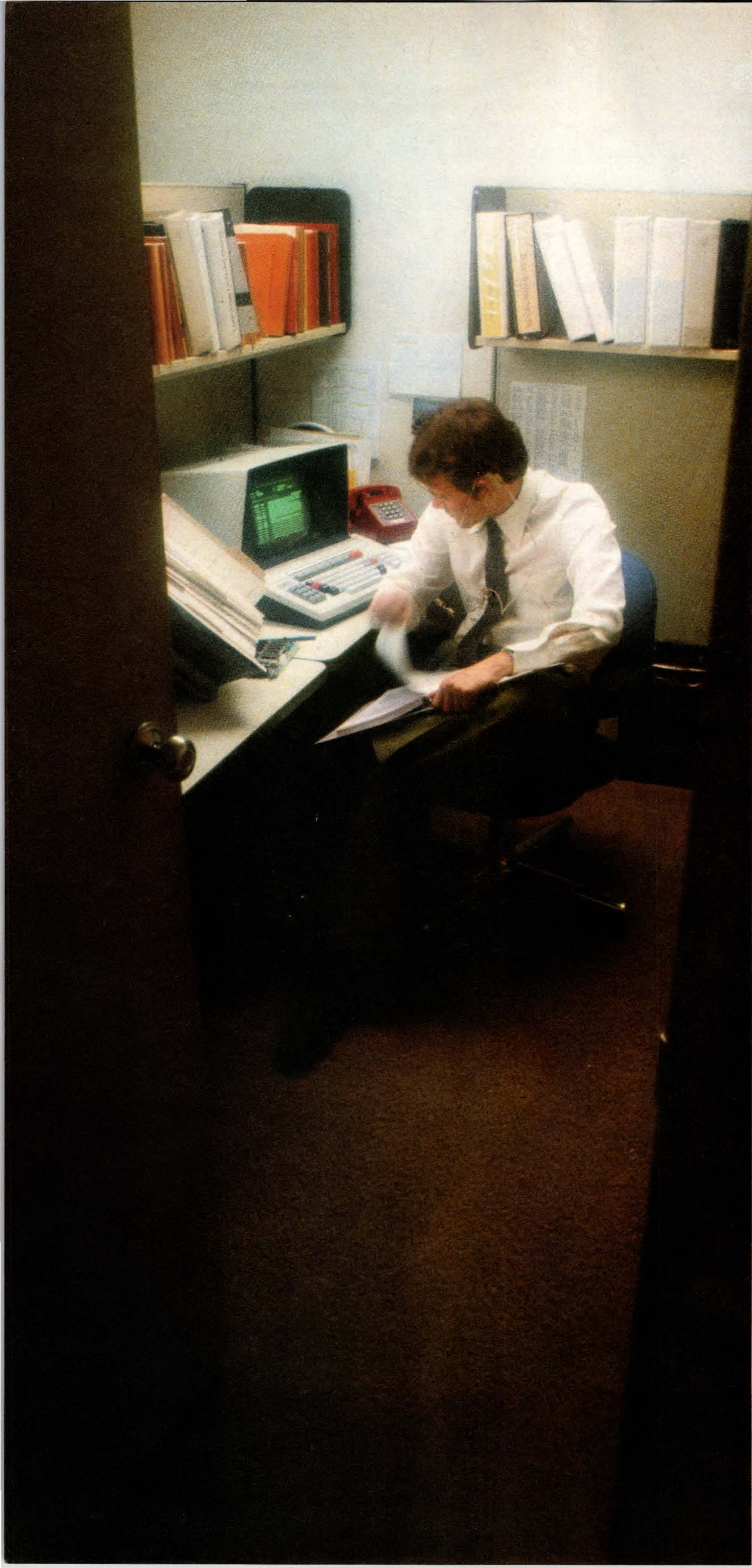
We're driving the drive market.

CIRCLE NO 114



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The RTC Answermen can also describe how TI's design automation system, with its series of checks and balances, minimizes errors and redesign. And they will explain the software tools available to ease and speed the design procedure.

◀ **At the ready:** The RTC Answermen in TI's Regional Technology Centers are equipped to provide virtually instantaneous information about TI logic arrays and a host of other TI semiconductor products. The RTCs are your most accessible entry point to TI's unmatched combination of product depth, design knowledge, and development tools that can result in the most cost-effective TI semiconductor solution for you.

Ask the RTC Answermen at Texas Instruments

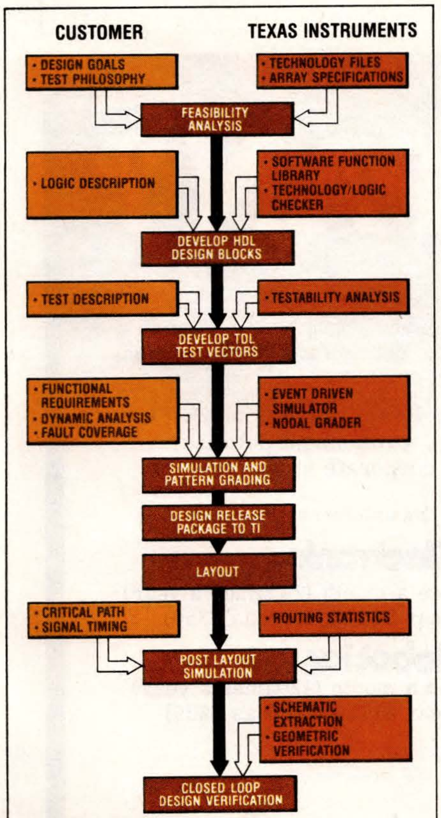
expect extensive design help logic array supplier?

What design training is available?

A five-day, design-level seminar is conducted regularly at the RTCs. This course will familiarize you with the techniques and capabilities of TI's design languages and automated software system.

During the course, you will learn TI's Hardware Description Language (HDL) and Test Description Language (TDL). They are used to define complex logic functions in a generalized format for compilation into a data base transferable into TI's design automation system.

The course also covers other tools available to you, including advanced simulation, design testability, design verification, and test-pattern grading.



Teamwork is essential to successful logic array design. As shown, the TI design process divides responsibilities for maximum contribution by both parties and eliminates many manual, error-prone tasks.

Fast, Efficient TI Logic Array Family

Array	Gates**	Technology†	Gate Delay	Gate Power	I/O Signals	Commercial/ Military
TAL002*	280	LPS	5.0 ns	1.25 mW	29	C
TAL004*	400	LPS	5.0 ns	1.25 mW	42	C
TAT004	400	STL	2.5 ns	600 μW	76	C/M
TAT008	800	STL	2.5 ns	600 μW	104	C/M
TAT010	1000	ASTL	1.0 ns	300 μW	88	C
TAT020	2000	ASTL	1.0 ns	300 μW	120	C/M
STL700	560	STL	3.0 ns	300 μW	61	M
SBP96700	1120	I^2L	11/15 ns	100 μW	96	M
SBP96600	2120	I^2L	11/15 ns	100 μW	140	M

*TAL Series Arrays are manually routed by you and schematically verified by TI with your software HDL model prior to prototyping.

**Usable gates

†LPS — Low-power Schottky

†STL — Schottky Transistor Logic

†ASTL — Advanced Schottky Transistor Logic

†I^2L — Integrated Injection Logic

When circumstances warrant, we'll conduct the seminar at your plant.

If you want to study on your own, appropriate documentation may be obtained from TI. This consists of a detailed Logic Array Designers Manual, data sheets of logic array characteristics, information packets on library-accessible, predesigned software functions, and related technology application notes.

Where can I get actual design assistance?

At TI's RTCs, home of the Answermen. TI engineers at the RTCs will evaluate your schematic at no charge. This evaluation includes assessment of your general performance requirements. Gate count. And associated I/O, as described by you.

The RTC will recommend the type of TI logic array best suited for your job (see table) as well as the appropriate package.

Each RTC has the facilities which you can use to describe your logic and prepare the HDL and TDL data base. If you prefer, the RTC will contract to do this work for you.

How readily can I access the design tools?

Everything at TI is done to make the design process as simple and as fast as possible. Access to TI's efficient design-automated system can be by terminals at the RTCs; by dial-up communication links from your plant, tied directly to TI's worldwide computing network. And by the Transportable Design Utility (TDU). The TDU allows you to perform your design work — utilizing the TI design software — at your own pace and on your in-house hardware.

The TDU, written in Pascal, includes the HDL compiler/syntax checker, TDL compiler, an interconnect rule checker, a design testability analyzer, and an event-driven logic simulator.

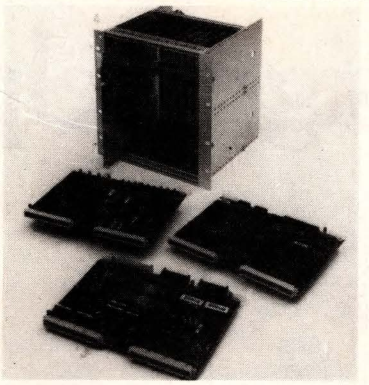
When should I start my design?

There's no better time than now. The RTC Answermen are standing by their Hot Line telephones (see listing opposite page) to answer your technical questions and assist you in taking advantage of the time and money savings inherent in TI's logic array design automation system. Or visit the RTC nearest you, or call your local TI sales engineer.

TEXAS INSTRUMENTS

CIRCLE NO 115

27-5030



VME-BUS BOARDS. Based on the 16/32-bit S68000 μP, these VME-bus modules are implemented in a 160×233.4-mm double-Eurocard format. For use in a VME-bus card cage or as a stand-alone single-board μC, the central-processor module employs an 8-MHz SCN68000 μP and provides optional memory management with the SC68451 memory-management IC; 48k bytes of ROM, PROM or EPROM; 8k bytes of high-speed RAM; two serial and one parallel ports; a 12-bit programmable real-time clock; and seven interrupt levels. Furnishing a 256k-byte high-speed RAM, the memory module supports 8-, 16- and 32-bit data transfers and accommodates 2-way interleaving. The disk-controller module supports as many as four 5¼- and 8-in. Winchester and floppy-disk drives. Functioning as an intelligent peripheral interface and DMA, it provides 200-nsec instruction-cycle time, flexible data formats and serial data rates to 8M bps. Providing comprehensive bus arbitration with four levels selectable for priority and round-robin modes, the system controller monitors system operation using a selectable watchdog timer, can detect improper address conditions and provides all system utilities, including a 16-MHz system clock and 4-MHz serial bus clock. CPU module, $2050; memory module, $2550; disk-controller module; $2200; system-controller module, $420. Delivery, 90 days ARO. **Signetics Corp,** Box 409, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 336

WINCHESTER CONTROLLER. Directly interfacing drives from more than 10 manufacturers, the iSBC 215 Generic Winchester Controller (GWC) combines the iSBC 215A open-loop controller, the iSBC 215B closed-loop controller and an ANSI X3T9/1226-standard interface controller on one Multibus board. Supporting as many as four 5¼-,

CIRCLE NO 118

WHEN YOU DESIGN OUR
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16K CMOS EPROM IN, EXTERNAL LATCHES OUT.

On-board latches. The new IM6716 UV ERASABLE 2K x 8 CMOS EPROM requires no external address latches. They're right on the chip. Replacing two external latches. Result: lower parts count, reduced board space and increased reliability. And that's just for openers.

Super-low power. You expect CMOS to be low power. But the IM6716 goes ordinary CMOS one better. Our synchronous design with on-board latches allows the IM6716 to operate at a standby Icc of only 100 micro amps. Half the competition's requirement. Without even considering the power draw of their external latches. Less parts. Less power.

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A pin-compatible family. 4K, 8K and now 16K CMOS EPROMs. Each with on-board latches. Each upward compatible with the next. Which means you can enhance your original design with a minimum of effort. Our 16K EPROM is also pin-compatible with our IM6316 CMOS ROM. When you reach high volume, simply move to the IM6316.

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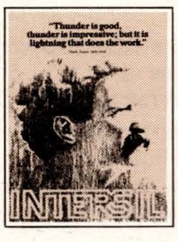

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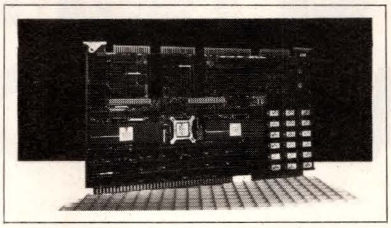
CIRCLE NO 119

8- or 14-in. Winchester drives, it appears to the Multibus as a standard software interface, regardless of drive type, permitting drive changes without rewriting software. The unit supports as much as 16M bytes of system memory and furnishes full-sector buffering, error correction using a 32-bit Fire code and automatic alternate-track assignment for defective tracks. For backup, the board provides two iSBX-bus connectors for floppy-disk and ¼-in.-tape Multimodule interfaces. $1500. **Intel Corp,** 5200 NE Elam Young Parkway, Hillsboro, OR 97123. Phone (503) 640-7147.

Circle No 337

SINGLE-BOARD COMPUTER. The Multibus-compatible HK68 furnishes an MC68000 8-MHz



μP with a 16-bit data bus, 16M-byte addressing, 17 32-bit registers, memory-mapped I/O and 14 addressing modes. Also provided are a 4-channel 16-bit DMA controller with internal 32-bit addressing; byte, word or long-word transfers to 4 MHz; programmable priorities; vectored interrupt support; and chained and unchained operational support. The segmented memory-management unit supports segment sizes of 256 to 16M bytes, separate supervisor/user-program/data memory areas and write protection. The board also features 256k or 128k of dual-access RAM with a National 8409 RAM controller, sockets for 64k of EPROM, a bus interface with 24-bit addressing and multimaster capability, two programmable serial-communications controllers, 8-bit Winchester and streaming-tape interfaces and three 16-bit counter/timer channels. $3895. **Heurikon Corp,** 3001 Latham Dr, Madison, WI 53713. Phone (608) 271-8700.

Circle No 338

PROCESSOR MODULE. Featuring the multiprocessing 16/32-bit VME bus, this Eurocard-format board provides a 10-MHz 16/32-bit 16032 μP with demand-paged virtual memory and Abort and Retry functions, an NS16082 memory-management unit and an NS16081 floating-point math processor. Compatible with the NS16000 family of system- and peripheral-control devices, it includes the 16KFORTH systems language in ROM with editor, assembler and compiler. Incorporating a multilevel operating system that can link other operating systems and compilers to a 16000-based system, it supports multiprocessing, multiuser and real-time process-control applications. Also available is a Z80 emulator and translator, which permit use of 8080 and Z80 code in a 16000-based environment. Available in February or March 1983. **Empirical Research Group Inc,** Box 1176, Milton, WA 98354. Phone (206) 631-4855.

Circle No 339

VOICE-SYNTHESIS MODULE. Containing a single-chip n-channel MOS IC that can, through stored allophones, synthesize any English phrase, the

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Back-up power you can call on anytime.

Phone system customers demand reliability. That's why major manufacturers of telecommunication systems are backing up their installations with Gates Energy cells.

Gates Energy cells deliver dependable back-up power that keeps your lines alive. They're rated at 2 volts with capacities at 2.5 Ah, 5 Ah, 12.5 Ah and 25 Ah. And they can be assembled into an endless variety of configurations.

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CIRCLE NO 121

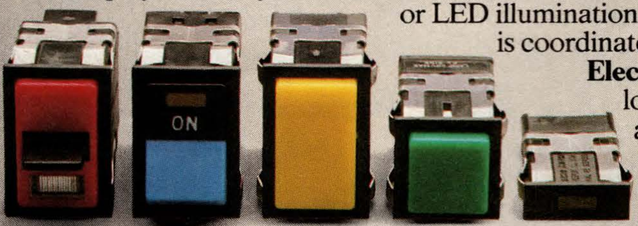
Courtesy of Gary Panton, Hughes Aircraft Company

Now, a complete, coordinated manual switch line that's ready for active duty.

Introducing the first complete MIL-qualified manual line. The new M22885 Series. It offers the same ergonomic excellence and high quality that make our Advanced Manual Line—AML—an industry leader. Plus, it's qualified to MIL-S-22885.

Functional flexibility. The line includes square and rectangular pushbuttons, and two- or three-position rockers and paddles, all in lighted or unlighted versions. They are complemented by indicators and annunciators; plus optional panel seals, barriers, mounting hardware and keylocks. And you'll get additional application flexibility because they're smaller and weigh less than other MIL-qualified manuals.

Display flexibility. You can choose from transmitted, projected or dead front hidden colors, and incandescent or LED illumination. Plus any legend or color you might need. And the line is coordinated, allowing you to maintain a uniform panel appearance.



Electrical flexibility. The M22885 Series handles anything from low-level loads to 15 amps, 125/250 VAC. Contacts are available in gold or silver. And they're the first MIL-qualified manuals to offer solid state versions. You'll get extra reliability and long life, because Hall effect integrated circuits replace touching contacts.

Cost-effective. These features combine with many others to make these manual switches cost-effective. For instance, they're priced lower than other MIL-qualified manuals. Features like snap-in mounting and single level termination lower installation costs. And you'll economize time and resources by taking advantage of our 35 years' experience supplying MIL-qualified products.

For manual switches that set new industry standards for quality and reliability, consider our MIL-qualified line. It's complete, coordinated, and ready for active duty.

For more information on our MIL-qualified manuals, and the locations of our sales offices and authorized distributors around the world, call 815-235-6600. Or write MICRO SWITCH, Freeport, IL 61032.

MICRO SWITCH
a Honeywell Division

CIRCLE NO 122

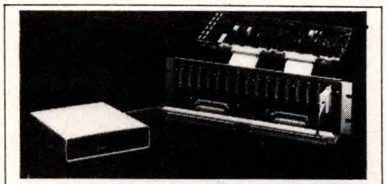
VSM2128-AL2 interfaces with any digital system utilizing a standard 15-pin card-edge connector. Ten TTL-compatible signals are used to select stored allophones. Utilizing its manufacturer's SPO256-AL2 single-chip speech synthesizer, the module operates from 4.6 to 7.0V. Audio output is filtered by an 8-pole Butterworth filter and amplified to drive an 8Ω load at 200 mW. $99. **General Instrument Corp,** 600 W John St, Hicksville, NY 11802. Phone (516) 733-3120.

Circle No 340

GPIB CONTROLLERS. TLC-488 GPIB talker/listener/controller interface boards allow a STD Bus system to control as many as 14 GPIB devices. The two boards can operate using interrupts or DMA, feature flexible port addressing and can transfer data at 200k bytes/sec. Each board requires 1A max of 5V dc power and presents no more than one TTL load to each STD Bus line. The boards come with a ribbon cable terminated in a GPIB connector and sample software. TL-488 talker/listener, $275; TCL-488 controller, $350. **Quasitronics Inc,** 211 Vandale Dr, Houston, PA 15342. Phone (412) 745-2663.

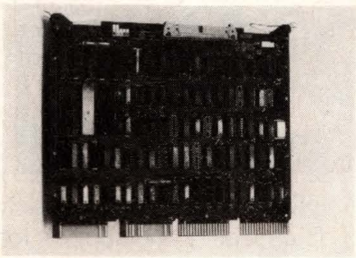
Circle No 341

BUS DRIVER. An integrated asynchronous terminal interface for DEC PDP-11 and VAX-11 computers, Series 11 BusDriver provides simultaneous support for local and remote terminals through the same multiplexer; connections for as many as 32



terminals via one Unibus slot; DH-11 capability and support for local terminals to 19,200 bps. Statistical multiplexing for remote terminals with error correction and data compression come standard, as does support for as many as 16 RS-232 interfaces. The basic unit includes a communications multiplexer, distribution panel and Micro800/2-NF data-concentrator-compatible remote - concentrator controller. From $5950. **Micom Systems Inc,** 20151 Nordhoff St, Chatsworth, CA 91311. Phone (213) 998-8844. TWX 910-494-4910.

Circle No 342



TAPE CONTROLLER. Mating as many as eight daisy-chained ¼-in. cartridge-tape transports with DEC LSI-11, -11/2 or -11/23 μCs, the quad-sized Model DQ320 provides eight times the storage capacity and six times the data-transfer rate of DEC-supplied cartridge transports. Interfacing the Data Electronics Model 3400 Funnel and Funnel interface-compatible transports from Epi, Perex and Qantex, it transfers data via DMA through an on-card FIFO buffer. A high-speed bipolar μC provides transport control, formatting and self diagnostics. During power-up, the system automatically checks the μC, buffer, data-path and CRC circuits to assure proper controller operation. $1017 (100). **Distributed Logic Corp,** 12800 Garden Grove Blvd, Garden Grove, CA 92643. Phone (714) 534-8950. TLX 681399.

Circle No 343

CONTROLLER / DEV - SYS CARD. The SYS-10 single-board STD Bus controller and self-contained development system suits such applications as data acquisition, process control and CAM. It runs on CAMBASIC, an optimized control version of standard BASIC. Hardware includes communication ports for a CRT terminal, printer and cassette; 8k on-board RAM; and an EPROM programmer. Other key features include an 8k interpreter/operating system; bit, byte and BCD manipulation commands; a run-time trace function, interactive debugging and text editor and a menu-driven utility library. The board accommodates master, slave or multiprocessor operation and operates from 5V. $485; OEM version with 2k RAM and without text editor, $380 (5). **Octagon Systems Corp,** 5150 W 80th Ave, Westminster, CO 80030. Phone (303) 426-8540.

Circle No 344

MULTIBUS I/O BOARDS. CBC 8730 Series features 32 single-ended/16 differential A/D and two D/A channels, a programmable-gain amplifier with 11 binary selectable gains of 1 to 1024 and a programmable offset option using one of the 12-bit D/A converters. True rms-to-dc conversion is software selectable; addressing is user selectable. The boards accommodate 4- to 20-mA current-loop inputs and outputs. The combination of programmable gain and offset permits dynamic autoranging of unipolar and bipolar signals of varying levels to achieve maximum resolution. When used in floating-point systems, the instrumentation amplifier provides an overall dynamic input range of 4,000,000:1. Common-mode rejection ratio equals 80 dB min. A Multibus interface comes standard; CMOS and TTL bus versions are also available. $1570 for CBC 8731-2. Delivery, stock to 6 wks ARO. **Diversified Technology Inc,** Box 748, Ridgeland, MS 39157. Phone (601) 856-4121.

Circle No 347

Cheap DC-DC converters can look like a great way to save money.

Until you start using them.

Then the special features show up: excess noise, poor regulation, thermal radiation, and more.

At Intronics, we spend a lot of time designing and manufacturing high reliability DC-DC converters from 1 to 100 Watts. We take great care in our component selection; we even make our own torroids and transformers. As a result, we can deliver DC-DC converters with the best price/performance ratio in the industry. And good old-fashioned reliability you'll come to depend on.

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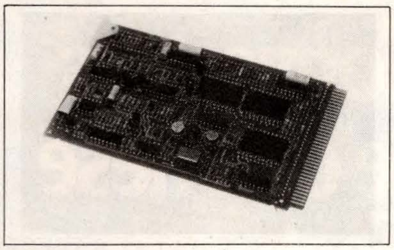


2400-BPS MODEM. Operating over leased or dial-up lines, Model R24LL serial synchronous DPSK modem can function in full-duplex (4-wire) or half-duplex (2-wire) modes. Housed on a 100×160-mm board, it is compatible with Bell 201 B/C, CCITT, V.26 A/B and V.26 bis standards and contains a CCITT-compatible V.27 scrambler function and a DTE interface, functionally equivalent to RS-232 and electrically compatible with LSTTL/CMOS. Also featured are transmitter - differential phase modulation and receiver-coherent phase detection, diagnostic outputs for eye-pattern generation and data-quality monitoring, a strap-selectable fixed-compromise equalizer, answerback tone generation and clear-to-send delay options. <$250 (OEM qty). **Rockwell International Electronic Devices Div,** Box C, Newport Beach, CA 92660. Phone (714) 833-4460.

Circle No 348

DAC. Compatible with IEEE-696 μC systems, Model SB-32-DA board provides 32 12-bit D/A output channels by multiplexing a 12-bit converter. Each channel has its own 16-segment waveform generator. The master processor sets 16 points on a waveform and 16 associated timing components by writing to the unit's RAM. It directly accesses the board's time-of-day counter, three 16-bit counters, two time-of-day alarm comparators, three 8-bit ports and eight frequency-counter channels. Five switchable unipolar and bipolar ranges are available, and each output drives a 1-kΩ load and exhibits 0.02% absolute accuracy. $825. Delivery, 6 wks ARO. **Digital Multi-Media Control,** 92972 River Rd, Junction City, OR 97448. Phone (503) 998-6575.

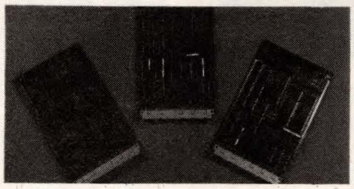
Circle No 349

DATA-ENCRYPTION BOARD. Utilizing a Western Digital chip to encrypt/decrypt data, the Encryptor provides a 64-bit data word and a 56-bit key word and features transfer rate of 1.3M bps. Level 0 software uses the NBS Electronic Code Book mode; higher levels use blocked cypher feedback. Secured data can be sent to any compatible system employing the Encryptor and supporting software. The S-100-bus board also features multilevel CP/M and OASIS file-encryption commands, 25-μsec encryption or decryption of eight bytes, switch-selectable I/O-port addressing, programmed I/O and switch-selectable vector interrupt priority. Apple, CP/M-86 and IBM Personal Computer versions are also available. Delivery, stock to 8 wks ARO. **Jones Futurex Inc,** 9700 Fair Oaks Blvd, Suite G, Fair Oaks, CA 95628. Phone (916) 966-6836.

Circle No 350

MOTOR CONTROLLER. A μP-based intelligent controller for stepper-motor drivers, SM-1 is RS-232 and STD Bus compatible and features 12,000-step/sec capacity with 65,536 steps per Move command. Providing isolated circuits that can drive 4-phase motors to 2.5A/phase, it can store as many as 200 user instructions. Equipped with three general-purpose outputs and two inputs, the 4½×6-in. unit comes with a 256-byte nonvolatile memory with 3-byte communications protocol to the STD Bus. $385. **Advanced Micro Systems Inc,** 9 Executive Dr, Hudson, NH 03051. Phone (603) 882-1447.

Circle No 351



VME-BUS MODULES. Expanding their manufacturer's VME8XXX line, these single-width Eurocard-format boards meet the VME-bus specification. VME8205 byte-wide memory board contains eight 28-pin sockets for a mix of 64k bytes of RAM or 128k bytes of ROM and provides access times of 62.5 to 500 nsec. Software configurable for synchronous or asynchronous operation to 880k baud, VME8300 quad serial-port board provides four serial ports; Bisync, HDLC or SDLC modes; DTR and CD modem-control lines and a spare timer for generating timed interrupts. VME8305 dual-parallel-port board furnishes 32 bits of configurable I/O, eight configurable handshake lines, polled or interrupt modes, two independent timers and a Centronics-compatible printer interface. Supporting as many as four 5¼- or 8-in. single- or double-density floppy-disk drives, VME8400 floppy-disk controller operates in polled or interrupt-driven modes. VME8205, $300; VME8300, $500; VME8305, $375; VME8400, $400. **Mizar Inc,** 2850 Bailey Rd, Newport, MN 55055. Phone (612) 459-2452.

Circle No 352

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MK 3880-4	8080A-2		

Find errors others miss.

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CP/M is a registered trademark of Digital Research Inc.
ISIS is a trademark of Intel Corporation.

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CIRCLE NO 77

SILICON SOFTWARE. The CP/M-86-based 80150 combines the iAPX 86-family-compatible version of Digital Research's CP/M operating system with essential operating-system hardware on one silicon chip. A processor extension compatible with the 8086, 8088 and 80186 µPs and incorporating the current 1.1 version of CP/M-86 stored in 16k bytes of on-board nonvolatile memory, the device provides key operating-system hardware functions, including timers and an interrupt controller. Resident CP/M-86 software includes the console command processor (CCP), basic disk operating system (BDOS) and the manufacturer's basic I/O system (BIOS). (CCP and BDOS are derived directly from CP/M-86.) Also included on chip are utilities such as diskette formatting, file transfer between devices and the capability of altering and displaying I/O-device and file status. BIOS contains system-dependent I/O drivers for various peripherals. $57.15 (1000). **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-5084.

Circle No 310

CONTOUR-PLOTTING PACKAGE. An interactive real-time contour - plotting system, CPS-1/G can be used on a wide variety of computers and output devices to create, analyze and edit contour maps for engineering, seismic, geological and other applications. Capable of working on a variety of batch contouring systems, this system is device and machine independent. Interactive features include display of raw data (control points), grids, base maps and contours and editing of control points by changing control-point locations, adding or deleting control points or changing their Z values. You can also edit grid values by changing one grid node and applying a smoothing filter to nodes within a polygonal region to fit the surrounding surface. The package also permits real-time contouring of the displayed or edited grid and interactive computation of statistical information. $25,000 with DI-3000 graphics-software package; $20,000 without. **Radian Corp,** Box 9948, Austin, TX 78766. Phone (512) 454-4797.

Circle No 311

GRAPHICS DRIVER. This package allows users of the manufacturer's computer-graphics software (which includes DI-3000, a core-based system, and GRAFMAKER, a high-level data-presentation package) to produce high-resolution 35-mm color slides and prints on the Xerox 350 system within 24 hrs. The slides can contain as many as 64 colors. You can choose among eight fonts of Helvetica type in light, medium or bold face and can control line thickness. Other features include program-selectable background color, 12 special marker symbols to identify graph points, nine text-justification points, shielding and optional drop shadows for text primitives. You can also generate a specially formatted Xerox plot file on your computer and send it to a Xerox Reproduction Center over phone lines or on magnetic tape through the mail. Driver license, $1000; slides, $15 to $30. **Precision Visuals Inc,** 250 Arapahoe, Boulder, CO 80302. Phone (303) 449-0806.

Circle No 312

CIRCLE NO 78

4 MILES UP, YOU CAN'T AFFORD A LESS RELIABLE PRESSURE TRANSDUCER.

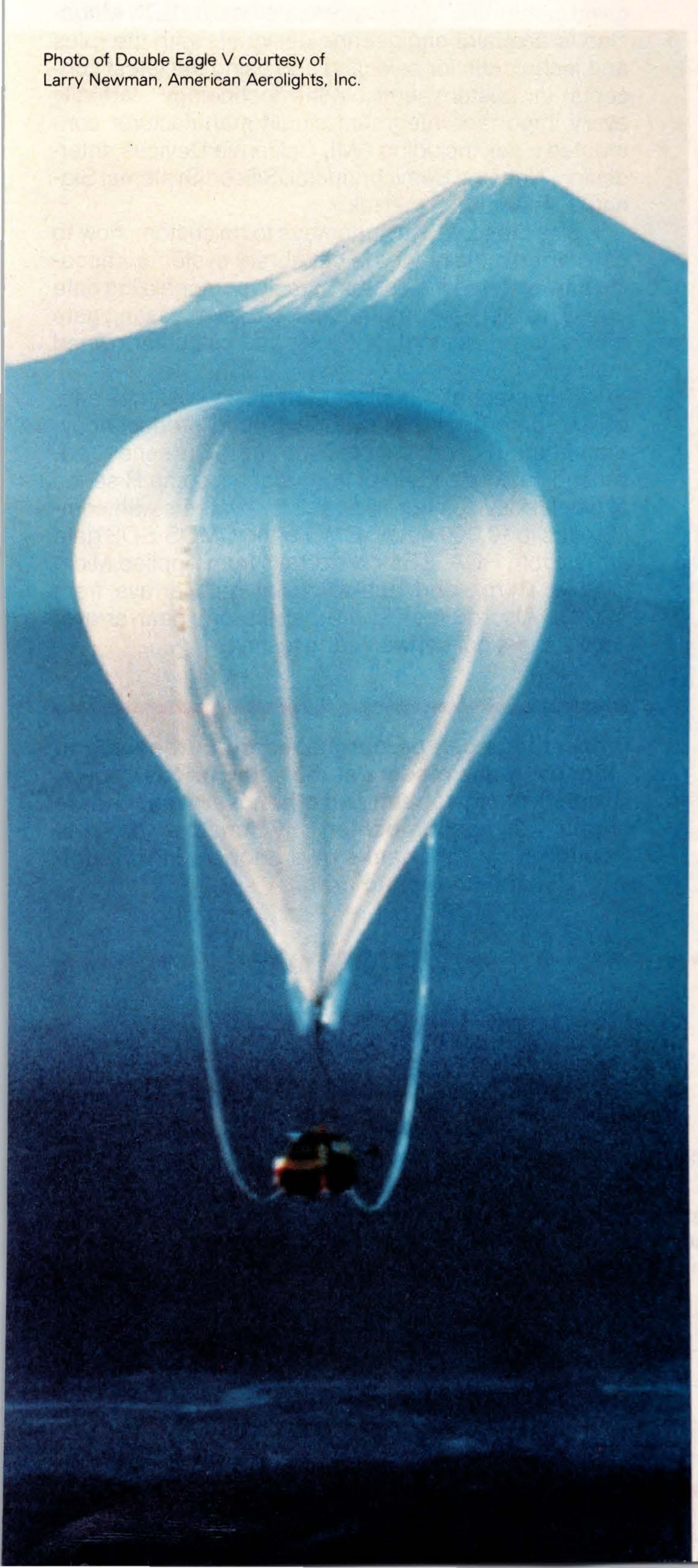

Photo of Double Eagle V courtesy of Larry Newman, American Aerolights, Inc.

Larry Newman and Ben Abruzzo put their lives on the line when they flew the Double Eagle V across the Pacific. One of the things they bet on was the reliability and accuracy of Foxboro/I.C.T. pressure transducers, which were an essential component in indicating Double Eagle's flight profile. We didn't let them down. And the Foxboro/I.C.T. pressure transducers proved to be among the most cost-effective systems on the balloon.

Affordable reliability. Every single Foxboro/I.C.T. pressure transducer is repeatedly tested at every level of manufacture. From wafer to fully signal-conditioned instrument. No other pressure transducer manufacturer makes that statement. By building in reliability, then testing in reliability, Foxboro/I.C.T. assures you maximum reliability in your own application.

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Proven technology. Foxboro/I.C.T. pressure transducers draw on the same I.C. technology that gave us the microprocessor. That technology combines high volume production with rigid quality control to give you maximum reliability and repeatability at minimum cost.

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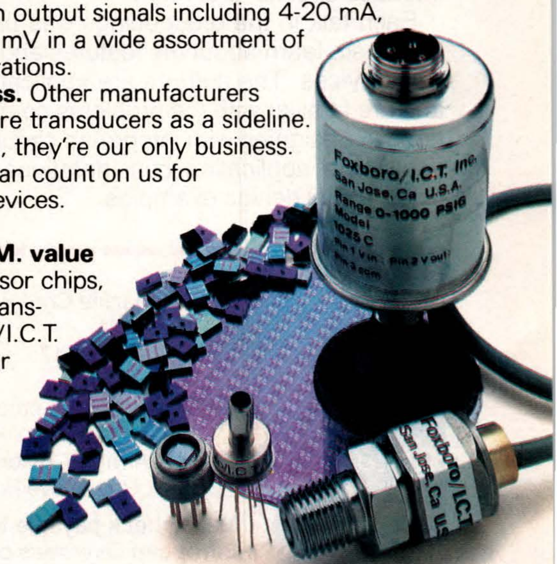

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For a free design guide to Foxboro/I.C.T. pressure transducers, call toll free or circle the Reader Service number below.

CIRCLE NO 79

COMPILERS. These OEM system-development packages produce code that can be linked and executed on the Motorola MC68000. One package resides on the Versados operating system; the other, on the RSX operating system for DEC PDP-11 computers. Versions of their developer's Pascal-2, the compilers support all capabilities of standard Pascal and conform closely to the draft proposed Pascal standard (ISO dp7185.1). Optional concurrent programming in Pascal, including true priority scheduling and capability of writing device drivers in Pascal, permits user programs to run without an operating system. The Pascal-2 MC68000 package comprises a native Versados compiler, an interactive source-level debugger, an execution profiler and other utilities running on Versados such as formatters and cross referencers. The Pascal-2 cross compiler includes a utility, XFR for transferring files from the RSX OS to Versados and back, and the native RSX compiler. Versados compiler and utilities, $5950; RSX cross compiler and transfer utility, $5950; with RSX native compiler and utilities, $7950; concurrent-programming package (including sources), $2000. **Oregon Software,** 2340 SW Canyon Rd, Portland, OR 97201. Phone (503) 226-7760.

Circle No 313

COLOR GRAPHICS. Version 1.0 of Draftsman for the IBM Personal Computer can generate standard graphs with minimum user input. Screen images can be printed on the IBM or Epson MX-80 printer, and data can be inputted in a variety of formats including VisiCalc DIF files. Graph formats include pie and bar charts (in addition to stacked and clustered bars), line graphs and scattergrams. One page accommodates multiple plots, and graph size and placement are variable. Figures can be drawn on the graph and saved. All input is via menus, and the software does not demand learning a special language or command syntax. The program runs with 64k of memory (128k is recommended), a color/graphics-monitor adapter and two disk drives. $200. **Starware,** 1701 K St NW, Washington, DC 20006. Phone (202) 466-7351.

Circle No 314

WATCH OUR DEVELOPING FAMILY OF TELEMETRY PRODUCTS.

Now Introducing d/pad Mark II

Loral Data Systems continues its lead in the development of PCM/PAM telemetry decommutation equipment with the introduction of d/pad Mark II. This is the latest in our d/pad series beginning with d/pad one through d/pad two and d/pad three, followed by the addition of analog/digital ports (ADP).

d/pad Mark II offers all the features of its three predecessors in one chassis while adding the capabilities of composite video output, independent bit sync and frame sync operation, data distribution, and real time limit check. The following options are available with the basic d/pad Mark II: Real-Time Limit Check Module; External Analog/Digital Ports; PAM Decommutation, Display and Simulation; Digital Ports (2 or 4); ASCII Interface with Selectable Baud Rates, 110 to 9600 (8); External Key board; IRIG-B Decoder; PCM Input Filter (fixed bit rates, 6-pole Bessel); Rack-Mount Kit (brackets, tilt slides, etc.); and Reusable Shipping Container.

For details about our new d/pad Mark II and an update on the latest activities in our engineering lab, call or write Chuck Stephens at Loral Data Systems, 9020 Balboa Avenue, San Diego, CA 92123. Phone: (619) 279-0411.

LORAL INSTRUMENTATION
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CIRCLE NO 82

ACCOUNTING SOFTWARE. A package of general-accounting software for accounts payable, accounts receivable, general ledger, inventory control, sales-order entry and word-processing applications, the Management Accounting Series (MAS) is designed for μCs running under CP/M, CP/M-86, MP/M II, TURBODOS, CROMIX or N/STAR operating systems. Written in CBASIC, CBASIC 86 and CB80, the software modules are interactive with one another and with WordStar word-processing software, the dBase II database-management package and MicroPlan financial modeling software. Each module can access another's data, so additional software modules and custom packages can be added without the need for rekeying data. Other features include suppress-menu facility, the capability of running on any display terminal using an 80-column format, automatic default and 9-level password protection for all programs. $3675 for complete package or $750 per module (except word-processing software, $450). **American Integrity Systems Inc,** 1415 E McFadden Ave, Suite A, Santa Ana, CA 92705. Phone (714) 973-4756.

Circle No 315

FORTH PACKAGES. These RAM-based FORTH and associated math packages run on the company's Aim-65, Aim-65/40 and RM-65 μCs. Two 4k ROMs provide a compiler, interpreter and assembler, a mass-storage operating system and a dictionary of approximately 300 subroutine procedure words. The language also contains single (16-bit)- and double (32-bit)-precision integer arithmetic. The associated math packages, each on one ROM, provide floating-point arithmetic and transcendental functions as extensions of the FORTH firmware. A run-time FORTH for the RM-65 allows FORTH programs developed on the Aim-65 to be executed by the RM-65 single-board-computer module. A FORTH program developed on the Aim-65/40 can be executed by an RM-65 system by using it as run-time FORTH in the SBC module. $35 for each package. **Rockwell International, Electronic Devices Div,** Box C, Newport Beach, CA 92660. Phone (714) 833-4802.

Circle No 316

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More people already own 1731 Linear IC Test systems than any other component tester. And now, with the addition of our new universal family board, our third in a series, it's more flexible than ever. In fact, the 1731 gives you the broadest component coverage of any benchtop system.

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CIRCLE NO 84

COMMUNICATIONS SOFTWARE. These enhanced communications capabilities for the developer's Personal Computer provide host-computer communications and emulation of the widely used 3270 and 3101 terminals. SNA 3270 emulation and RJE support software permit the Personal Computer to act as a terminal that can communicate with a host system in one of two modes, supporting Systems Network Architecture (SNA) 3270 or SNA 3770 Remote Job Entry (RJE). 3101-terminal emulation furnishes nearly complete emulation of the company's 3101 display terminal, Model 20, according to user-selected options in specification files and transmission of ASCII format files to and from host computer and local diskette storage. It also permits conversion of ASCII format diskette files to and from binary format. Asynchronous communications support (Version 2.0) allows use of Personal Computers as asynchronous TTY ASR 33/35 terminals without additional programming and permits one Personal Computer to transfer program and data files to another. SNA 3270 emulation and RJE support, $700; 3101-terminal emulation, $140; asynchronous communications support, $60. Communications package available now; other packages, in January 1983. **IBM System Products Div,** Box 1328, Boca Raton, FL 33432. Phone (305) 998-6007.

Circle No 317

C COMPILER. An improved version of its developer's C compiler, this software requires only a 48k system and runs under I/OS, UNI/OS, MultiI/OS, CP/M or CDOS. A 3-pass true compiler, it can directly produce 8080 object code in relocatable format or assembler source code. Outputs can be Microsoft relocatable object code, the developer's relocatable object code, Microsoft M80 Assembler source or the firm's SAL Assembler source. Symbolic definition of global variables, functions and source line numbers is provided. Standard package features include longs, all C operators and statements, structures, unions and initializers, and disk selection for overlays and library Include. **InfoSoft Systems Inc,** 25 Sylvan Rd South, Westport, CT 06880. Phone (203) 226-8937.

Circle No 318

MICROPROCESSORS
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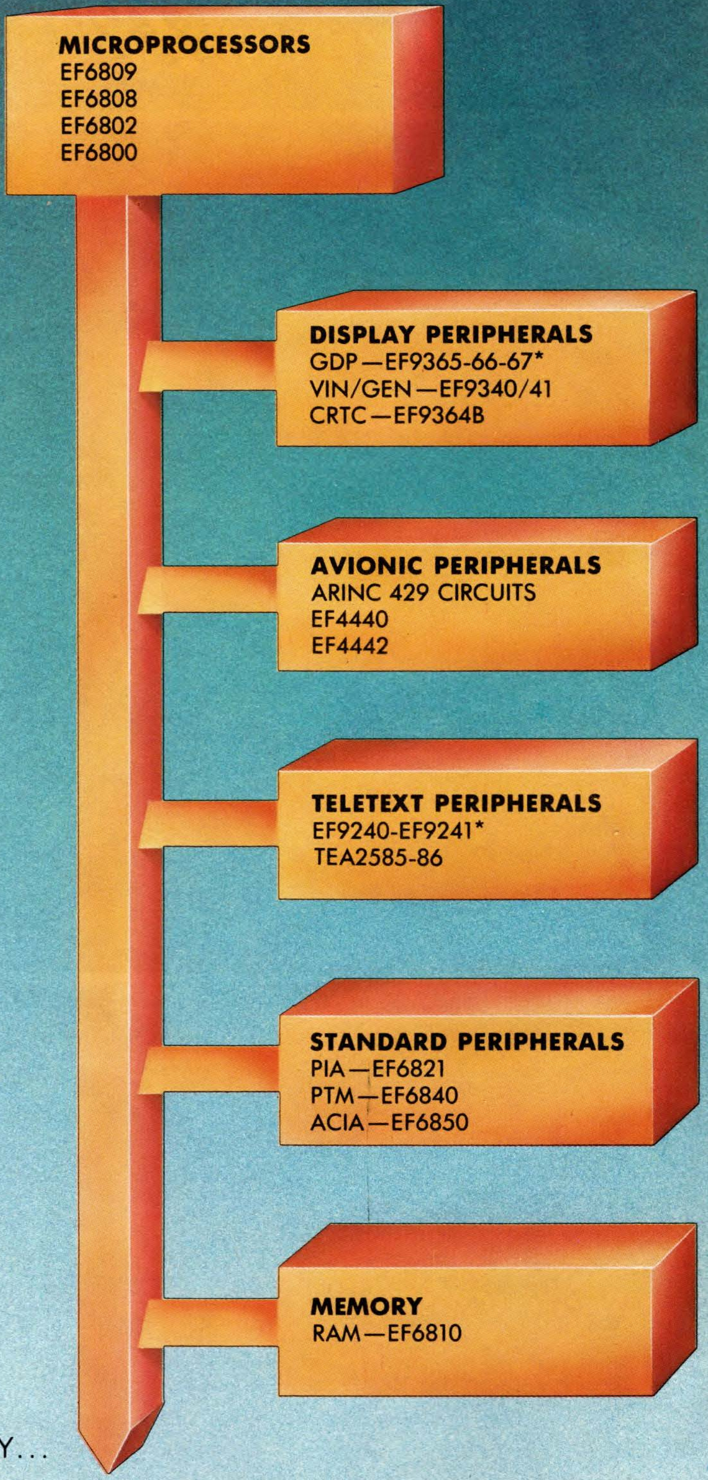
Thomson-EFCIS, a world leader in MOS technology, introduces its 6800 Family of Microprocessors and innovative peripherals, meeting industry demands for high-technology, quality products at competitive prices.

Product Family	Type Number	Description	
MICROPROCESSOR (Motorola Second Source)	EF6800 EF68A00 EF68B00	8 BIT MPU	1 MHz 1.5 MHz 2 MHz
	EF6802 EF68A02 EF68B02	8 BIT MPU + CLOCK + RAM	1 MHz 1.5 MHz 2 MHz
	EF6808	8 BIT MPU + CLOCK	1 MHz
	EF6809 EF68A09 EF68B09	HIGH PERFORMANCE 8/16 BIT MPU	1 MHz 1.5 MHz 2 MHz
DISPLAY PERIPHERALS (First Source)	EF9365 EF9366 EF9367*	GRAPHIC DISPLAY PROCESSOR	512x512 Pixels 512x256 Pixels 1024x416 Pixels
	EF9340/41	ALPHANUMERIC & SEMI-GRAPHIC DISPLAY PROCESSOR	
	EF9364B	ALPHANUMERIC CRT PROCESSOR	
AVIONIC PERIPHERALS (First Source)	EF4440*	ARINC 429 TRANSCEIVER LOGIC INTERFACE	
	EF4442	ARINC 429 MULTI-CHANNEL BUFFER RECEIVER	
TELETEXT PERIPHERALS (First Source)	EF9240	CHANNEL & PAGE SELECTOR	
	EF9241	CHANNEL & PAGE SELECTOR	
STANDARD PERIPHERALS (Motorola Second Source)	EF6821 EF68A21 EF68B21	PIA PERIPHERAL INTERFACE ADAPTER	1 MHz 1.5 MHz 2 MHz
	EF6840 EF68A40 EF68B40	PTM PROGRAMMABLE TIMER MODULE	1 MHz 1.5 MHz 2 MHz
	EF6850 EF68A50 EF68B50	ACIA ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER	1 MHz 1.5 MHz 2 MHz
MEMORY (Motorola Second Source)	EF6810 EF68A10 EF68B10	128x8 STATIC RAM	1 MHz 1.5 MHz 2 MHz

*In development



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CIRCLE NO 87

SYMBOLIC DEBUGGER. For VMS, RSX-11, IAS, RT-11, RSTS and UNIX operating systems running on PDP-11 and VAX hosts, SI 8086 tests and modifies Intel 8086 and 8088 software. A program user first creates and assembles a program on a CRT or other terminal attached to a DEC computer. Once the program correctly assembles, rather than down line-load the object files to an emulator or to a prototype board-level system, the user can test the generated program from the same terminal. The debugger permits immediate access and execution of the assembled program, whereas an emulator requires a 10- to 20-min wait to load a large program. $5000 when leased or purchased with a corresponding assembler. **Boston Systems Office,** 469 Moody St, Waltham, MA 02154. Phone (617) 894-7800. TWX 710-324-0760.

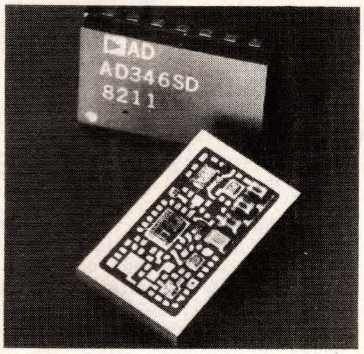
Circle No 319

MENU INTERFACE. Providing the capabilities of Bell Labs's UNIX in a menu-driven format, this menu-driven command interpreter (shell) enables nonprogramming personnel to run UNIX-based applications such as word processing, accounting, file and data management and system administration. For use on its manufacturer's 16-bit 8086- and 68000-based μCs, the shell features compatibility with any RS-232 terminal, menu-customization capability, a utility to simplify user administration procedures and three sets of menus designed for end users and system administrators and designers. Simplifying UNIX operation, the system provides menu selection and prompts for additional information when required, at the bottom of the screen. Sophisticated users, on the other hand, can execute UNIX commands directly by prefacing them with an exclamation point or by entering the standard UNIX shell or C shell directly. $995 as part of the firm's XENIX/UNIX implementation. **Altos Computer Systems,** 2360 Bering Dr, San Jose, CA 95131. Phone (408) 946-6700.

Circle No 320

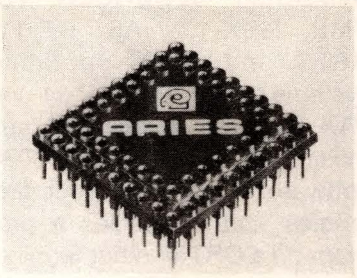
OPERATING SYSTEM. For the MC68000 μP, REGULUS is C-language source-code compatible with Bell Labs's UNIX V6, V7 and System III. It provides superset enhancements that include real-time tasks, file-record locking and dynamic allocation of file index records. Also furnished are automatic configuration, flexible- and/or hard-disk support, user-defined signals and a terminal line editor. The multiuser, multitasking system supports real-time priority-driven tasks and intertask communications and doesn't require a memory-management unit. It uses 128k bytes of main memory; an OEM version for dedicated applications needs 32k of memory for the system kernel. Binary single copy, $1550; source code, $12,000. **Alcyon Corp,** 8716 Production Ave, San Diego, CA 92121. Phone (714) 578-0860.

Circle No 321



SAMPLE/HOLD AMP. The AD346 features 2-μsec max guaranteed acquisition time to ±0.01%, 500-mW max power consumption and a droop rate of 0.5 mV/msec max. Pin compatible with industry-standard Model 346, it specs 1.4-MHz typ full-power −3-dB bandwidth, 50V/μsec slew rate and 400-psec aperture jitter. Operating in unity-gain inverting mode, it guarantees maximum initial gain and offset errors of ±0.02% FSR and ±3 mV, respectively. Total offset error over temperature is guaranteed at ±20 mV max, while total gain error over temperature specs at ±0.05% max. Rated specifications apply over 0 to 70°C for the J grade and −55 to +125°C for the S grade. Maximum feedthrough is guaranteed at ±0.02% FSR, while sample/hold switching-transient amplitude equals <40 mV pk typ. Housed in a 14-pin hermetically sealed ceramic DIP, the device requires ±12 to ±18V power supplies and draws +18 and −10 mA max quiescent current. $56 and $84 (100) for J and S grades, respectively. **Analog Devices Semiconductor,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 935-5565.

Circle No 353



PIN-GRID-ARRAY SOCKET. Designed to accept components requiring other than the conventional DIP matrix, this unit comprises 64 collet-style contacts positioned on 0.100-in. centers and arranged in a square matrix. They accept 0.018- to 0.025-in. pins. A multilevel pin grid helps reduce insertion force. $0.03 to $0.08 per position. **Aries Electronics Inc,** Box 130, Frenchtown, NJ 08825. Phone (201) 996-6841.

Circle No 354

CIRCLE NO 89

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LB and KB Series Illuminated Switches are designed to help you upgrade the beauty and efficiency of your panels.

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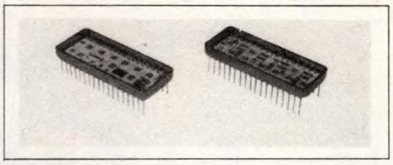
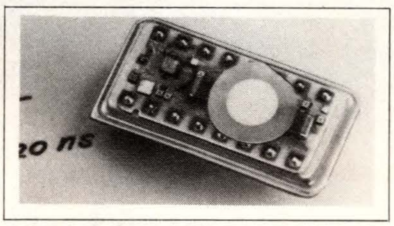
CIRCLE NO 90



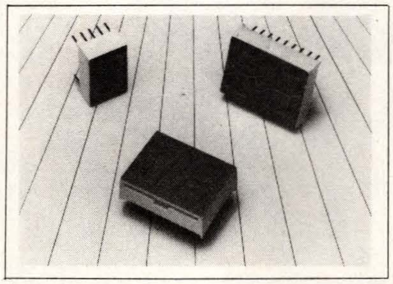
14-BIT S/D, R/D CONVERTER. The multiplexed HMSDC-8700 converts four synchro or resolver channels to 14-bit digital data and includes a 4-channel input-processor module and a central-converter module. The hybrid-circuit design's algorithm achieves accuracies of ±4.6′±½ LSB and 150-μsec/channel max conversion time. All common synchro and resolver line-to-line voltages and frequencies are available. Signal and reference input channels can be interconnected and hybrid and discrete versions interchanged in any combination. As many as 100 input channels can be accommodated when operated at 60 Hz. Random-access capability allows you to select only the desired channels. $1275. Delivery, stock to 90 days ARO. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 355



CRYSTAL OSCILLATORS. 8003 Series dual-output devices feature initial accuracy of ±0.01% of specified frequency at 25°C and ±0.01% of initial accuracy over operating temperatures spanning −55 to +200°C. Each unit's rectangular-wave output is compatible with 5V Schottky and 5 to 15V CMOS loads. Output frequencies span 500 kHz to 16 MHz. User-specified operating voltages equal 5, 10, 12 and 15V. Two standard models, the 8003-1.1085 and 8003-.640, spec outputs of 369.5 kHz and 1.1085 MHz and 213.3 kHz and 0.640 MHz, respectively. Packaged in a 14-pin-DIP welded metal case, both units are priced at $172 (100). **Custom Devices,** 4246 E Wood St, Phoenix, AZ 85040. Phone (602) 268-1371. TWX 910-951-4203.

Circle No 356

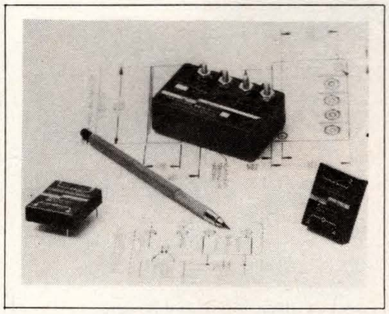


7-SEGMENT LEDs. MAN6400 Series green units are available in 2-digit common-anode and common-cathode forms with right-hand decimal; 1½-digit common-anode and common-cathode versions with overflow/polarity indicator and right-hand decimal; and single-digit common-anode and common-cathode designs with right-hand decimal. Furnishing a gray face and neutral segment color to enhance on/off contrast, they spec 710-μcd/segment minimum luminous intensity at 60-mA peak forward current and 1:6 duty factor. Rise time equals 12 nsec typ; viewing angle, 150°. **General Instrument Optoelectronics,** 3400 Hillview Ave, Palo Alto, CA 94304. Phone (415) 493-0400

Circle No 357

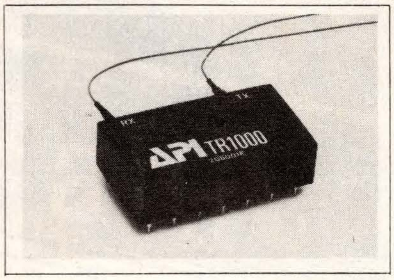
REED RELAY. Available with axial or pc-board terminals, the TG Series device measures 0.64 in. long and 0.25 in. in diameter and provides coil-voltage ratings of 5, 6, 12 and 24V. Designed with end coil or side coil and with options for handling a 0.7-in. pc-board mounting, the Form 1A unit can switch 0.5A as well as signal loads. Switch rating specs at 10 VA (100V dc max and 0.05A dc). $1.22 (1000). **Standex Electronics,** 4538 Camberwell Rd, Cincinnati, OH 45209. Phone (513) 871-3777.

Circle No 358



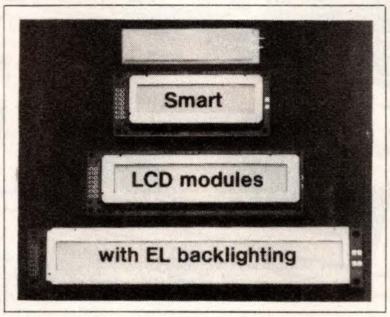
SOLID STATE RELAYS. Opto-switch Series units are totally encapsulated and suit use in high - shock and severe-temperature environments. All inputs are optoisolated (1500V ac, $10^{10}\Omega$ dc), and turn-on is synchronized with load-voltage zero crossing to minimize RFI. Operating voltage spans 24 to 140V ac with 250V pk repetitive voltage. The 12-OPC Series specs 3 or 4A current rating for pc mount, continuous at 25°C. 12-OTM Series units, a heavy-duty industrial panel-mount version, are rated at 6 to 40A. Operating frequency spans 47 to 65 Hz; temperature range, −40 to +100°C. Control voltages are TTL compatible with reverse-polarity protection of inputs. Delivery, 4 to 6 wks ARO. 12-OPC Series, $7.50 (100); 12-OTM Series, $18. **Applied Electro Technology International,** 2220 S Anne St, Santa Ana, CA 92704. Phone (714) 556-6570. TWX 910-595-1797.

Circle No 359



ELECTRO-OPTIC TRANSCEIVER. A fiber-optic transmission interface using an LED source and PIN-diode photodetector, Model TR1000 is pc-board mountable, provides fiber strain relief and furnishes either single or differential inputs that permit interfacing to ECL, TTL and CMOS. It accommodates any digital data rate from dc to 24M bps with receiver sensitivity of −40 dBm, or any analog rate from dc to 12 MHz with optical dynamic range >27 dB. Measuring 2.8×1.5×¾ in., the unit suits use with standard 50-μm-core/125-μm-cladding optical fiber and also with 100/140-μm fiber. $150. **American Photonics Inc,** Milltown Office Park, Rte 22, Brewster, NY 10509. Phone (914) 278-9224.

Circle No 360



LCD MODULES. PC151X/152X Series units consist of a liquid-crystal display, a CMOS driver, a CMOS LSI controller and an optional electroluminescent lamp with half life of 7500 hrs. Six standard models are available, with 16×1, 24×1, 40×1, 16×2, 24×2 and 40×2 characters. Features include sunlight readability, user-programmable characters, 5V dc power supply, 5×7 and 5×10 dot-matrix character fonts with cursor, and μP-compatible 4- or 8-bit data-bus interface. All control, refresh and display functions are executed by a dedicated on-board controller. The devices can display the full 160-character JIS font set plus 32-character special font sets. $44.25 to $100.50 (100). **Photochemical Products of California,** 18031 Susana Rd, Rancho Dominguez, CA 90221. Phone (213) 603-0400.

Circle No 361

Championship Price/Performance By The Contender!

HS 574

Complete, 12-bit, 25μSec A/D Converter with μP interface.

$34.50! (100's)

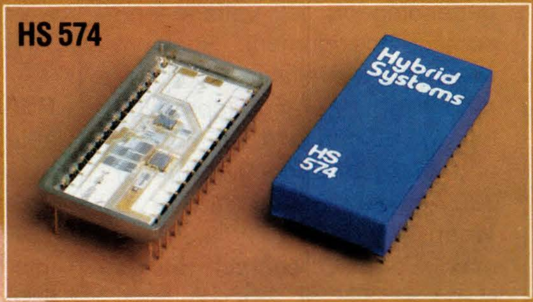
The Hybrid Systems 574 gives you real punch at a winning price. A complete 12-bit analog to digital converter, it features reference, clock and tri-state outputs for direct 150 nSec interface to 8 or 16-bit microprocessor buses. This state-of-the-art converter combines advanced linear bipolar, CMOS LSI and multi-metal thin film technologies. And we made it work!

You get 25μSec conversion, guaranteed linearity over temperature, for a mere 600 mW of power. The HS 574 is available in an economical plastic package for commercial applications. Or get the complete, all metal, hermetically sealed MIL version, which is specified over the full military temperature range and complies with 883B.

Call today. You'll see why the Contender wins on price/performance every time.

Hybrid Systems Corporation 22 Linnell Circle, Billerica, MA 01822; (617) 667-8700.

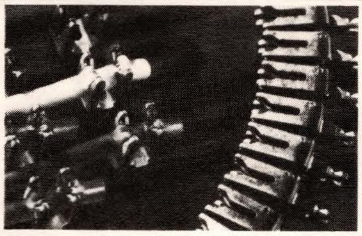
Another Technical Knockout by the Contender



Hybrid Systems
CORPORATION

CIRCLE NO 93

Components & Packaging



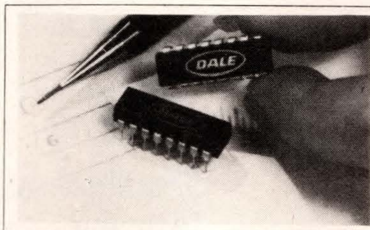
PC-BOARD TERMINAL. Quadra-Mate terminates discrete wires after wave soldering via single ending, daisy chaining or on-board jumping. This low-profile (<¼ in. high) brass connector has tin-over-copper plating and uses 4-slot insulation-displacement technology to provide redundant contact and strain relief for 30- to 24-AWG solid, stranded and fused wires. Measuring 0.100 in. wide, it requires 0.120×0.130 in. of board area. The device is available singly or in strip form for semiautomatic or automatic insertion. **AMP Inc,** Harrisburg, PA 17105. Phone (717) 564-0100.

Circle No 362

REED RELAY. Available as either an open or covered unit, the UL-recognized JRW Series device accommodates pc-board mounting via wave soldering. Compatible with automatic cleaning systems, it features standard coil voltages of 3, 5, 6, 9, 12, 15 and 24V dc. Nominal coil power spans 50 to 833 mW, depending on coil voltage and contact arrangement. Rhodium contacts are available in configurations of 1 Form A (spst NO) through 2 Form C (dpdt). Form A and B contacts handle 10W at 200V dc max, 0.5A dc max or 10 VA at 140V ac max and 0.35A ac max. Form C contact ratings stand at 3W at 28V dc max, 0.125A dc max or 3 VA at 28V ac max and 0.09A ac max. Maximum operate time (including bounce) at 25°C equals 2 msec for Form A and Form B contacts and 2.5 msec for Form C contacts. Maximum initial contact resistance for Form A and Form B contacts equals 0.15Ω; it's 0.2Ω for Form C contacts. 1 Form A version, $3.43 (100). Delivery, 6 to 8 wks ARO. **Potter & Brumfield Div AMF Inc,** 200 Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2260.

Circle No 363

LCD. Model FE2201 features 3½ 0.2-in.-high characters (seven segments), three decimal points, a colon, plus/minus sign and an overrange arrow. Designed for multimeters and available in transmissive, reflective and transflective modes, it comes with DIP connector pins attached or in a pinless version for use with elastomeric connectors. Measuring 1.6×0.70 in., the unit specs operating temperature of −20 to +55°C or −20 to +80°C. Red, blue and green readouts are optional. $10.60 (100). **AND,** 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916. TWX 910-374-2353. **Circle No 364**

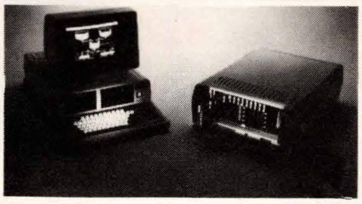


RESISTOR NETWORKS. Available in 14-pin (seven isolated resistors) and 16-pin (eight isolated resistors) models, Type TDP devices utilize Nichrome thin-film construction and are housed in a molded case with 0.150-in. max above-board height. They spec a resistance range of 100Ω to 100 kΩ in standard tolerances of 2, 1, 0.5 and 0.1%. Standard temperature coefficient equals ±25 ppm/°C; ±10 ppm/°C is available. Individual resistors have a 0.1W max power rating at 25°C. Total package power rating equals 0.7W max. $2.10 (500) for 7-resistor model with 1.0% tolerance and 10-kΩ resistance. **Dale Electronics Inc,** Dept 860, Box 609, Columbus, NB 68601. Phone (402) 371-0080.

Circle No 365

DATA-ACQUISITION MODULE. Measuring 3×4.5×0.375 in., Model DAS-5716 comprises a complete data-acquisition system, including a 16-channel (eight differential) multiplexer, programmable-gain instrumentation amplifier, track-and-hold amplifier, and a successive-approximation-type A/D converter with 16 bits of resolution and 3-state output buffers. It also includes all required timing and control circuitry and its own precision reference supply. The instrumentation amplifier achieves gains of 1 to 2000 with one external resistor. You can select either single-ended or differential input configurations and can specify unipolar or bipolar operation (jumper selectable on the 12-bit model). Throughput specs at 40 kHz max on the 12-bit model, 10 kHz max on the 14-bit version and 2.5 kHz max on the 16-bit device. 12 bits, $300; 14 bits, $695; 16 bits, $975. **Intech Microcircuits Div,** 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. TWX 910-338-2213.

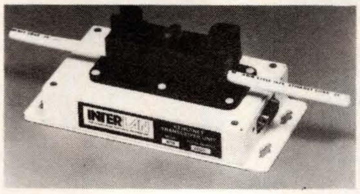
Circle No 366



MEASUREMENT-AND-CONTROL SYSTEM. Macsym 350 combines flexible I/O options, a system console and an intelligent measurement-and-control front end. The system console comprises an 8086 CPU, an 8087 math coprocessor, 128k bytes of RAM, an intelligent graphics controller, a 5¼-in. 320k-byte floppy-disk drive and a communications controller. Six I/O slots handle communication and memory options. The front end contains an 8088 μP, 256k bytes of memory, an ADIO controller and 16 slots for I/O cards. The system accommodates as many as 512 channels. You can choose from a library of 32 I/O cards, including isolated and nonisolated analog and digital inputs and outputs, IEEE-488 controller, RS-232/422 and 20-mA current-loop communications, speech synthesis, interrupt, setpoint alarm, strain gauge, thermocouple, RTD, milliamps, millivolts and volts. The system controls as many as 18 tasks simultaneously and acquires 33,000 samples/sec max in Burst mode. $9990. Available in February. **Analog Devices Inc,** 2 Technology Way, Norwood, MA 02062. Phone (617) 329-4700.

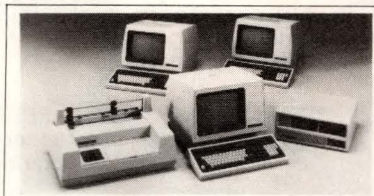
Circle No 367

ETHERNET TRANSCEIVER. Via a nonintrusive coax-cable tap, the NT10 connects and disconnects from an operational Ethernet local-area network without disrupting network communications. Its tap contains



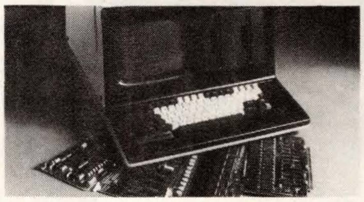
probes that pierce the cable to achieve an electrical connection. Should the device make an excessively long transmission, its jabber-control logic electrically disconnects it from the coax. Triple-protection design ensures that no single or double component failure degrades the communication of other Ethernet stations. Loopback and heartbeat features permit users to send transmissions that verify proper circuit operation. The unit provides 500V ac electrical isolation between the Ethernet coax and the transceiver cable, eliminating noise-inducing ground loops. $290. **Interlan Inc,** 160 Turnpike Rd, Chelmsford, MA 01824. Phone (617) 256-5888.

Circle No 368



COMPUTER SYSTEMS. Based on a single-board CPU using the manufacturer's TMS 99000 μP, the five Business System 300 Series units provide 128k bytes of error-correcting main memory (expandable to 512k bytes) and 5M to 43M bytes of storage. Maximum disk storage equals 172M bytes and is achieved by linking four 43M-byte disk subsystems. The family uses the manufacturer's DX10 operating system. Its software application packages include general ledger, accounts payable, accounts receivable, inventory control, payroll and word processing. Each computer includes a video-display terminal with a detachable keyboard and a 12-in.-diagonal screen that displays 80 columns×24 lines. $9995 to $21,800. **Texas Instruments Inc,** Box 202146, Dallas, TX 75220. Phone (512) 250-7305.

Circle No 369



DESKTOP CONTROLLER. Based on the 8/16-bit MC6809 μP, the Exorset 35 accommodates such programming techniques as structured programming, position-independent code, re-entrant routines and real-time operations. Features include full-size ASCII keyboard and 16 user-assigned function keys and a 9-in. CRT that simultaneously displays 22 lines of 80 or 16 lines of 40 upper- and lower-case characters and a full 320×256-dot graphic image. Three versions are available: the 351-0 has no floppy-disk drives; the 351-1 provides one double-sided mini-floppy-disk drive for 164k bytes of mass storage; and the 351-2 includes two disk drives for 328k bytes of mass storage. Each includes 2k bytes of dynamic RAM for CRT character refresh, 56k bytes of dynamic RAM and three strappable sockets that can be configured for 1k, 2k, 4k or 8k ROMs or EPROMs. 351-0, $3305; 351-1, $4070; 351-2, $4675. **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. Phone (602) 244-5714.

Circle No 370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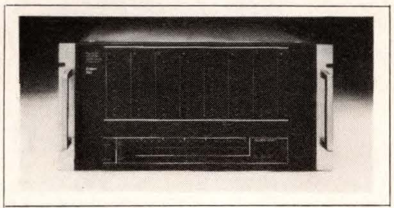


DATA-CONVERSION SYSTEM. The DSC-200 suits applications requiring the digital analysis and reproduction of sound. It contains a remote audio console, 16-bit A/D and D/A converters and four DMA interfaces. An extensive FORTRAN library, menu-selectable diagnostics and Record and Playback programs ensure rapid installation and use. The unit accommodates 16 analog input or output channels. Stereo record and playback, full-duplex operation (simultaneous record and playback), and multiprocessor configurations are optional. $16,500. Delivery, 60 days ARO. **Digital Sound Corp,** 2030 Alameda Padre Serra, Santa Barbara, CA 93103. Phone (805) 963-8951.

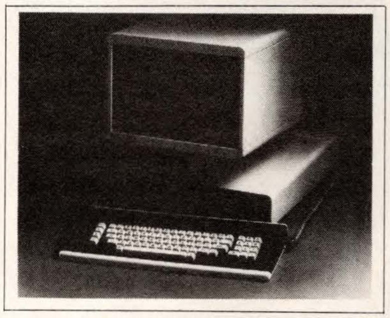
Circle No 371

INK-JET PRINTER MODULE. The 125-color Spectrum 2000 delivers full-page prints in <40 sec. By sending 12 TTL-compatible signals over a 26-pin ribbon cable and adding a power supply, you can incorporate this device into color-copying or color-printing devices. It recognizes 24 commands for establishing operating modes, controlling paper movements and transmitting color information. With head movements of 108 raster inches per sec max, the unit provides 150-dots/in. horizontal density. A maximum horizontal image size of 12 in. provides more than 1800 controllable pixels. Vertical density of 85 dots/in. is standard. Self contained and field replaceable, the unit specs life rating >6000 hrs MTBF and head reliability $>10^{10}$ operations. Other commands include built-in self test, signature analysis and alignment. **PrintaColor Corp,** 5965 Peachtree Corners East, Norcross, GA 30071. Phone (404) 448-2675.

Circle No 372

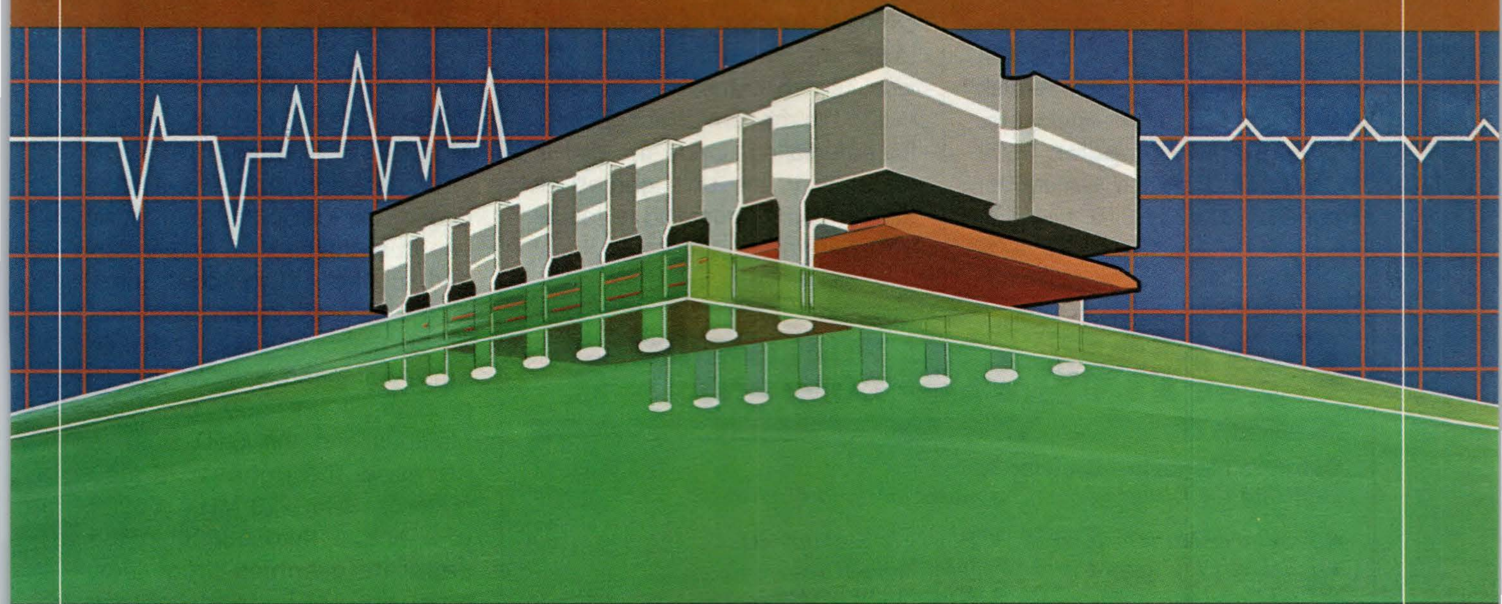
PROGRAMMABLE CONTROLLER. AutoMate 15 accommodates as many as 64 I/O channels in any combination of pairs and as many as 1000 relay-ladder logic elements in its application memory. The memory incorporates nonvolatile E^2PROM and NOVRAM; no battery backup is required for memory retention upon loss of power. Average scan time equals 2 to 3 msec, and maximum scan time with fully loaded memory and 64 I/O is 7 msec. Standard functions include internal coils (64 coils for use in interlocking logic), timing (16 timers max, 32,767 0.01-sec ticks), counting (eight counters max, 32,767 counts each) and shift register (four shift registers max, user-assignable length). Standard line voltages equal 115/230V ac, 50/60 Hz; an optional 24V dc power supply is available. Incoming power is fused within the head, and the fuse is replaceable from the front. $1000 to $1500 for typical configuration. Delivery, 8 wks ARO. **Reliance Electric,** 4900 Lewis Rd, Stone Mountain, GA 30083. Phone (404) 938-4888.

Circle No 373



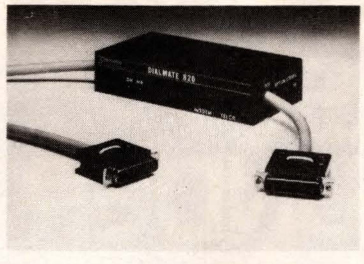
16-BIT MINICOMPUTER. Compatible with IRIS, BITS, IOS, BLIS/COBOL and other operating systems, the Ardent 15 features a master-port visual display, detached keyboard, virtual console, real-time clock and a parallel line-printer controller. It operates at 400-nsec cycle time and features 64k bytes of RAM, expandable to 256k bytes. The unit accepts interrupts from peripheral controllers wired in a serial priority structure and accommodates DMA operation. It supports four additional user terminals or serial devices through RS-232 ports. Two standard 15×15 slots accommodate compatible peripheral controllers and interfaces, including a variety of multiplexers, disk controllers and magnetic-tape controllers. A detached DIN-standard keyboard comes with 128 ASCII characters and features a coil cable and a 10-key numeric keypad. $4990. **Ardent Computer Products,** 2259 Via Burton, Anaheim, CA 92806. Phone (714) 870-7660.

Circle No 374



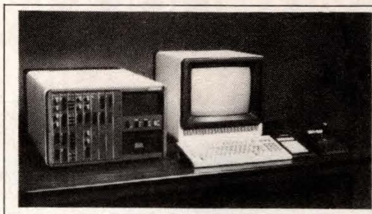
16-BIT μC. The E-1 system, a single- or multiuser unit based on the 8086-1 μP, operates at 10 MHz with no Wait states. The MP/M-86-based μC can handle as many as 10 remote workstations. It comes standard with 512k bytes of dynamic RAM and is upgradable to 1M bytes. A minimum configuration includes two 8-in. single-sided, double-density floppy-disk drives with formatted capacity of more than 1M bytes. Options include a fixed 14-in. hard-disk drive with 30M-byte capacity that can be mounted within the system's enclosure; a streaming cartridge-tape drive; double-sided, double-density 8-in. floppy-disk drives; and a desk enclosure. $5995. **Euclid Computer,** 3699 W 240th St, Torrance, CA 90505. Phone (213) 373-9316.

Circle No 375



MODEM AUTODIALER. Dialmate 820 replaces the RS-232C cable that normally connects a modem and a data terminal. It receives serial dialing commands from a terminal keyboard and returns its dialing status for screen display. The direct-connect modem accesses the telephone line through the device, which transfers the data call to the modem after successful autodialing. Once the call is under way, the unit ignores all dialing commands and is totally transparent. It adapts to local telephone switching systems by automatically selecting either a DTMF tone or a rotary-type pulse dialing method. The unit's serial operating system supports 10 dialing commands. $249. **Cermetek Microelectronics Inc,** 1308 Borregas Ave, Sunnyvale, CA 94086. Phone (408) 734-8150.

Circle No 376



COMPUTER SYSTEM. Model MC-500 is a 32-bit, 16M-byte virtual-memory, real-time UNIX-based minicomputer that suits use in real-time data acquisition and control, high-speed data analysis and graphical-format applications. It uses multiple processors and a triple bus (a proprietary MC-500 bus, the Multibus and the STD Bus) to increase throughput. It also features twin 10-MHz 68000 μPs and a third 68000 in the separate graphics processor, plus an 8M-instructions/sec 2901 bit-slice processor for data acquisition and control. The user-programmable data-acquisition and control processor accommodates 2M bytes/sec of I/O analog and digital data. The system acquires analog data at 1M samples/sec with 12-bit resolution and provides a high-resolution raster-graphics system with either monochrome or color monitor. As many as four graphics units can be supported. <$28,000. **Masscomp,** 543 Great Rd, Littleton, MA 01460. Phone (617) 486-9425.

Circle No 377

The AD524. You can't build or buy a better I/A. And you won't believe the price—under $10!

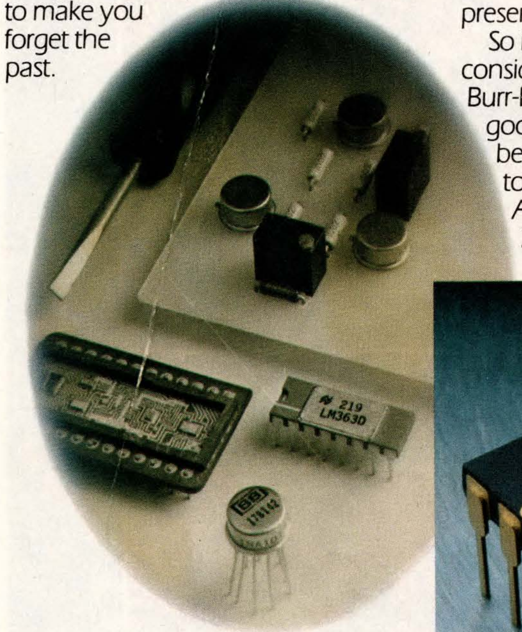
The struggle to come up with the right I/A for your application is over. Never again will you have to design around two or three op amps and a handful of resistors, or pay the high price of a hybrid, or settle for a monolithic IC with less-than-satisfactory specs. Our new monolithic AD524 gives you all the performance and functionality you'll ever need in an I/A. And you can get it all at a price that's designed to make you forget the past.

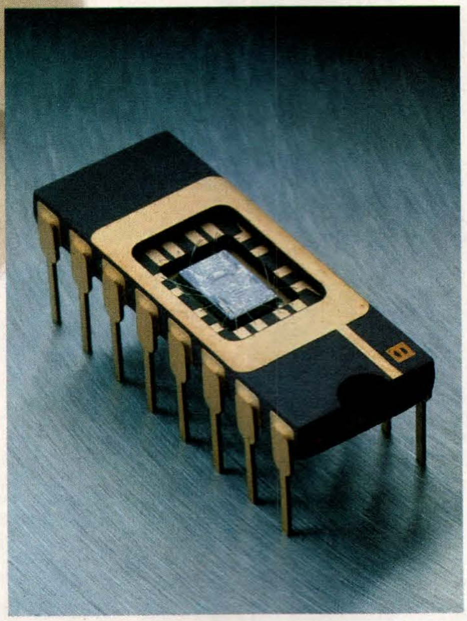
The AD524 has the best specs attainable in an I/A, whether you're talking monolithic, hybrid, or discrete. Nonlinearity to ±0.003%. Input offset voltage drift of ±0.5 μV/°C. Gain error of ±0.02%. Common mode rejection of 130 dB. 0.3μV peak-to-peak low frequency noise. Your dream specs are now a reality!

And the AD524 couldn't be easier to use. Pre-trimmed on-chip gain resistors give you pin-strappable gains of 1, 10, 100, or 1000. The AD524's inputs are internally protected against over-voltage (power on or off), eliminating the need for external diode clamps. And sense and reference inputs let you make sure that the output is accurately presented to the load.

So if you're still rolling your own, or considering the National LM363 or the Burr-Brown INA101, find out just how good an instrumentation amp can be. Call Don Travers or Doug Grant today at 617-935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

ANALOG DEVICES





The instrumentation amp that makes all else obsolete.

Analog Devices, Inc., One Technology Way, Norwood, MA 02062; Headquarters: 617-329-4700; California: 714-842-1717, 408-947-0633; Illinois: 312-653-5000; Ohio: 614-764-8795; Pennsylvania: 215-643-7790; Texas: 214-231-5094; 713-664-6704; Washington: 206-251-9550; Belgium: 031/37 48 03; Denmark: 02/84 58 00; France: 01/687 34 11; Holland: 016/20 51080; Israel: 052/28995; Italy: 02/68 98 045; Japan: 03/263 6826; Sweden: 08/282740; Switzerland: 022/31 57 60; United Kingdom: 01/941 0466; West Germany: 089/514010.

CIRCLE NO 97

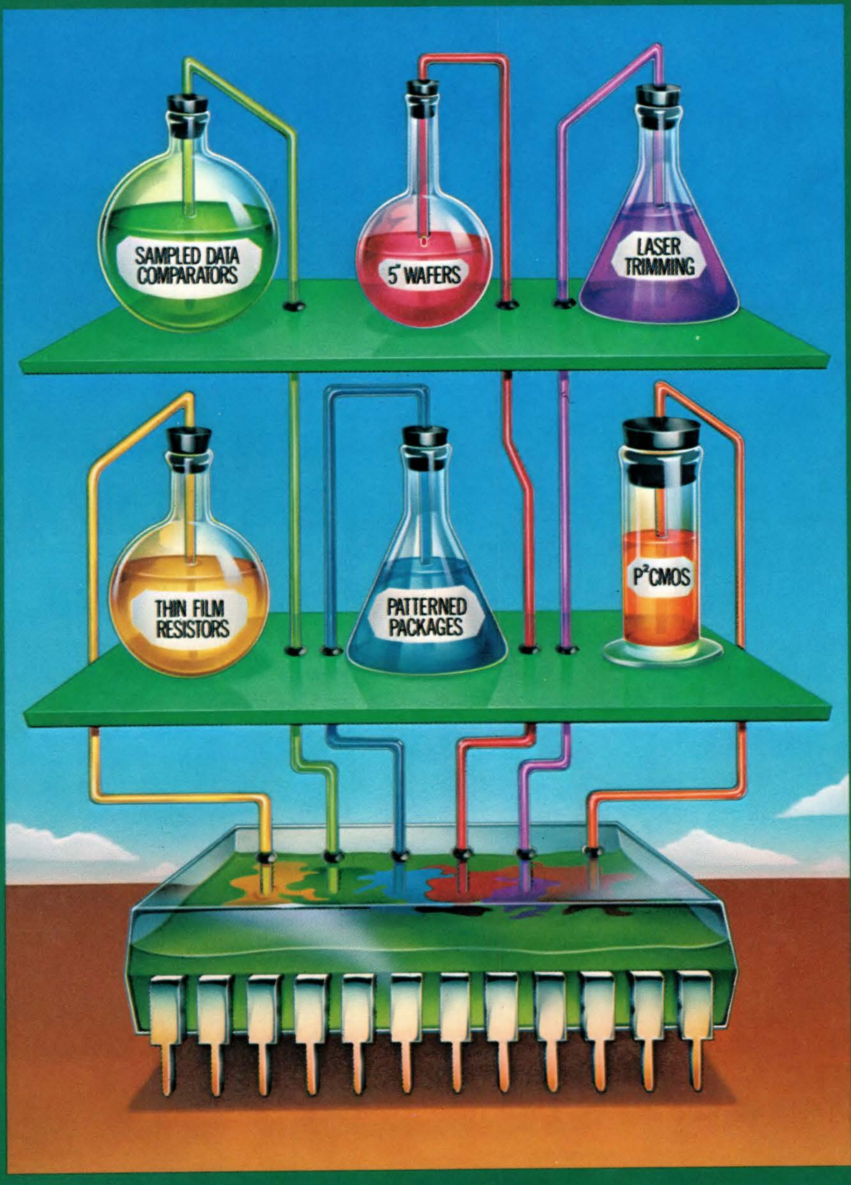
NATIONAL ANTHEM®

SPECIAL ISSUE

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

Six advanced technologies yield the best cost/performance in A/Ds and D/As.

A UNIQUE COMBINATION OF ADVANCED DESIGN AND PRODUCTION TECHNOLOGIES REDUCE DATA ACQUISITION COSTS.



8-bit analog/microcontroller interfacing made easy

Low cost 10-bit A/Ds

World's best, complete 12-bit DAC

Free Data Acquisition literature

SPECIAL DATA ACQUISITION ISSUE

SPECIAL ISSUE

Six advanced technologies yield the best cost/performance in A/Ds and D/As.

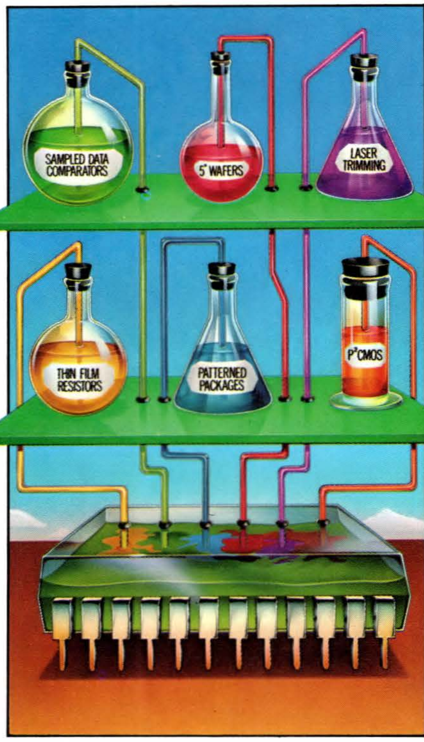
Thin-film resistors, laser trimming, sampled data comparators, P²CMOS,™ patterned packages, and 5" wafers lead the list of technological advances that add up to the utmost in data acquisition cost/performance.

Applied to Data Acquisition, Practical Wizardry means designing and producing the lowest cost A/Ds and D/As for the performance levels that are in greatest demand.

To do this, only National utilizes all six of these advanced design and production technologies: thin-film resistors, laser trimming, sampled data comparators, P²CMOS, patterned packages, and 5-inch wafers.

Laser-trimmed thin-film resistors. By incorporating laser-trimmed thin-film resistors, their 10- and 12-bit A/Ds and D/As offer unsurpassed precision and temperature coefficients.

Sampled data comparators eliminate fatal A/D design flaws. Many of National's A/Ds also utilize sampled data comparators. The result: high speed at low overdrive is designed into each chip, with oscillations, noise, and offset designed out.



P²CMOS: higher speed, lower cost. P²CMOS, National's own double-poly, silicon-gate process, increases device speeds in several ways.

For example, P²CMOS features shallow junction depths which reduce junction capacitance. Also, the higher circuit density afforded by two levels of interconnect provides higher speeds at lower cost.

The best things come in patterned packages. The reliability and cost-effectiveness of their hybrid Data Acquisition components is further enhanced by using patterned packages.

Since these packages also allow automated die attach and wire bonding, production costs (i.e., unit costs) are driven even further down while at the same time increasing reliability.

5-inch wafers: yields go up, unit costs go down. Further advancing the leading edge of production technology, National's unique five-inch wafer lines are driving unit costs straight through the floor.

When it comes to Data Acquisition, Practical Wizardry is synonymous with cost/performance.

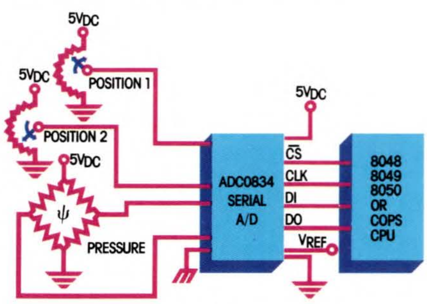
P²CMOS is a trademark of National Semiconductor Corporation.

Cost-effective analog/microcontroller interfacing made easy.

The industry's first binary 8-bit serial A/D family makes microcontroller interfacing a snap.

Until now, binary 8-bit A/Ds all used parallel I/O. Parallel is fast, but it takes up more than it's share of I/O pins, PC board space and traces.

But now there's a cost-effective alternative that emphasizes ease of use and high accuracy at low prices.



TYPICAL BLOCK DIAGRAM FOR A FOUR-CHANNEL DEVICE

It's the ADC0831 8-bit serial A/D converter family. It's an industry first from National, the cost-performance innovators in Data Acquisition/Conversion technology.

Complete microcomputer and microcontroller compatibility. National designed the ADC0831 family to be easily used with any microcomputer device, including their entire 8048/49/50 family, and the NSC800 microprocessor.

The ADC0831 family also complies with National's MICROWIRE™ serial data exchange standard for the simplest interface to their COPS™ family of single-chip microcontrollers.

The numbers tell the story. To make it even more convenient to use, the ADC0831 family offers:

- A total unadjusted error of ±½ LSB and ±1 LSB.
- No full-scale or zero adjust.
- 0-, 2-, 4-, or 8-channel analog multiplexer options.
- A single 5 V_{DC} supply requirement.
- A 32 μsec conversion time.
- A 0V to 5V input range with a single 5V power supply.

Nothing else available even comes close in ease-of-use, board economy, and cost/performance.

For more information on the ADC0831 family of 8-bit A/Ds, check boxes F9 and G0 on this Anthem's coupon.

Another affordable innovation from the Practical Wizards.

MICROWIRE and COPS are trademarks of National Semiconductor Corporation.
*U.S. price only.

PRODUCT SUMMARY TABLE

P/N	ANALOG INPUT CHANNELS	100 UNIT PRICE*
ADC0831CCN†	1	$2.70
ADC0832CCN†	2	$3.10
ADC0833CCN‡	4	$3.20
ADC0834CCN†	4	$3.20
ADC0838CCN†	8	$3.35

†Reference requirement is equal to the analog input range.
‡Reference requirement is equal to one half of the analog input range.

A graphic comparison of the world's best, complete 12-bit DACs.

The totally self-contained DAC1280A and DAC1285A Series offers lower power and higher speed than the industry standard DAC80s, DAC85s and DAC87s.

National Semiconductor now offers the highest performance complete 12-bit DACs: their new DAC1280A and DAC1285A Series.

The new industry standard is here.
These fast converters settle to full scale accuracy in only 300ns (current mode) and 2.5μs (voltage mode), while dissipating only 500mW.

The DAC1280A, for example, guarantees maximum linearity error of ±½ LSB over the entire 0°C to 70°C temperature range. It also guarantees a ±¾ LSB differential non-linearity and a precise 6.2V reference (±2%) over temperature.

In addition, all specs are guaranteed over a ± 11.4V to ± 15.75V supply voltage range.

All these DACs complementary binary logic inputs—also guaranteed over temperature—are compatible with TTL and CMOS logic levels.

Self-contained reliability and price.
National's design utilizes a monolithic wafer laser-trimmed bipolar DAC, a precision thin film laser-trimmed reference, and a high speed precision op amp (voltage version only). This permits a variety of cost advantages as well as reliability advantages.

Initial savings stem directly from a less complicated, and hence less costly, manufacturing process. But more importantly, the standard IC construction technique results in reliability enhancements over the other DAC80s. And that means dependable performance over the long term.

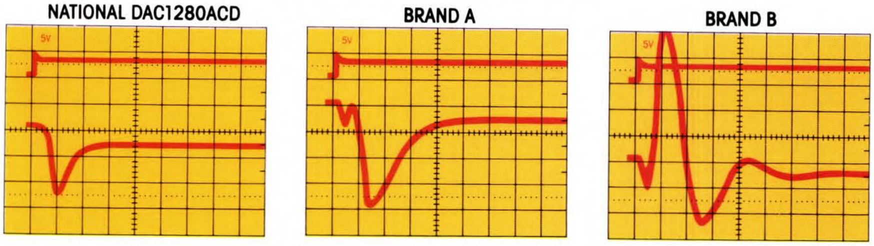
For complete details on the world's best, complete 12-bit DACs, check box number 57 on this issue's National Archives coupon.

12-BIT DAC CROSS-REFERENCE TABLE.

NATIONAL P/N	ALTERNATIVE P/N
DAC1280AC	DAC80-CBI-V; DAC80Z-CBI-V
DAC1280AC-I	DAC80-CBI-I; DAC80Z-CBI-I
DAC1285C	DAC85-CBI-V
DAC1285AC	DAC85LD-CBI-V
DAC1285A	DAC87-CBI-V

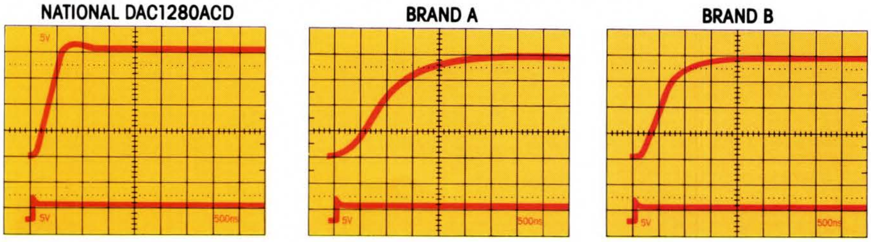
SETTLING TIME FOR 1 LSB CHANGE

NATIONAL DAC1280ACD — BRAND A — BRAND B



FULL SCALE SETTLING TIME −10V TO +10V

NATIONAL DAC1280ACD — BRAND A — BRAND B



First class performance at economy prices in 10-bit A/Ds.

The lowest cost successive approximation 10-bit A/D.

Data conversion applications that don't require speeds faster than 200μs don't require A/Ds that cost more than the ADC1001 or ADC1021.

It's the fastest 10-bit monolithic CMOS device on the market. Plus it has the lowest cost of any 10-bit device at its speed.

With a non-linearity of ±1 LSB, the ADC1001/21 cuts the need for additional power supplies by requiring only a single 5V power supply at 7.5 mW.

Like many of National's other A/Ds, it's easy to interface, requiring no external logic for microprocessor interfaces.

The ADC1001 is designed for easy 8-bit bus interface. The ADC1021, with its 10-bit TRI-STATE® outputs, is ideal for wider buses.

The ADC1021CCN is available in a 24-pin (.6" center) DIP and is priced at $15.95* in quantities of 100 and up. The ADC1001CCN is packaged in a 20-pin (.3" center) DIP and is priced at only $14.95* in quantities of 100 and up.

With price/performance like this, it's no wonder that the ADC1001 and ADC1021 are finding their way into all sorts of critical field applications from medical instrumentation to hand-held battery-operated devices.

To get more on the ADC1001 and ADC1021, just check box G1 on this Anthem's coupon.

For speeds of 200μs and up, they offer first class performance at economy prices.

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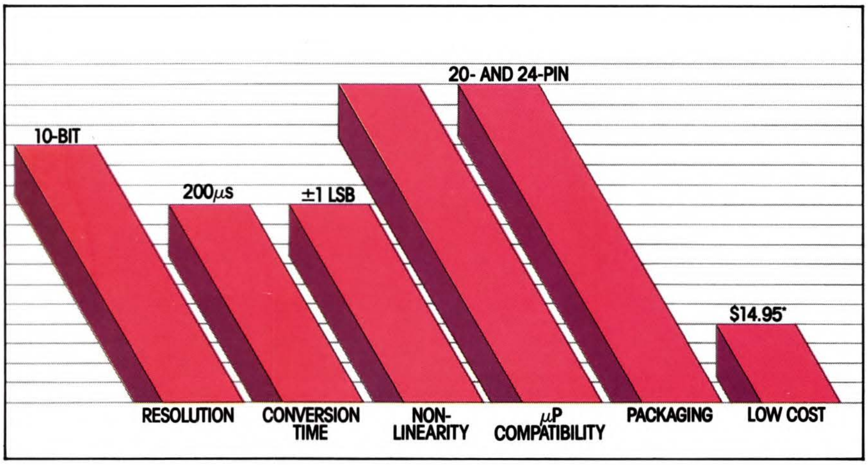

The complete line of top-of-the-line A/Ds.

A/D CONVERTERS

PART NO.	RESOLUTION (BITS)	CONVERSION TIME	COMMENTS	ABSOLUTE ACCURACY (MAX)
ADC0800	8	50μs	Bipolar Input	±2 LSB
ADC0801	8	110μs	Differential Input	±¼ LSB
ADC0802	8	110μs	Differential Input	±½ LSB
ADC0803	8	110μs	Differential Input	±½ LSB
ADC0804	8	110μs	Differential Input	±1 LSB
ADC0805	8	110μs	Ratiometric Operation	±1 LSB
ADC0808	8	100μs	Includes 8-Channel MUX	±½ LSB
ADC0809	8	100μs	Includes 8-Channel MUX	±1 LSB
ADC0816	8	100μs	Includes 16-Channel MUX	±½ LSB
ADC0817	8	100μs	Includes 16-Channel MUX	±1 LSB
ADC0820B	8	1.2μs	Includes T/H Function	±½ LSB
ADC0820C	8	1.2μs	Includes T/H Function	±1 LSB
ADC0831B	8	32μs	8-Pin Serial I/O	±½ LSB
ADC0831C	8	32μs	8-Pin Serial I/O	±1 LSB
ADC0832B	8	32μs	2-Channel Serial I/O	±½ LSB
ADC0832C	8	32μs	2-Channel Serial I/O	±½ LSB
ADC0833B	8	32μs	4-Channel Serial I/O	±½ LSB
ADC0833C	8	32μs	4-Channel Serial I/O	±1 LSB
ADC0834B	8	32μs	4-Channel Serial I/O	±½ LSB
ADC0834C	8	32μs	4-Channel Serial I/O	±1 LSB
ADC0838B	8	32μs	8-Channel Serial I/O	±½ LSB
ADC0838C	8	32μs	8-Channel Serial I/O	±1 LSB
ADC1001C	10	200μs	Differential Input	±1 LSB
ADC1020C	10	200μs	Differential Input	±1 LSB
ADC1080	10	18μs	With Reference and Clock	±½ LSB
ADC1210	12	26μs	Low Power	±½ LSB
ADC1211	12 (10)	26μs	Low Power	±1 LSB
ADC1280	12	22μs	With Reference and Clock	±½ LSB
ADC3511	3½-Digit	200ms	Integrating μP Compatible	0.05%
ADC3711	3¾-Digit	400ms	Integrating μP Compatible	0.05%
LM131	V-F	N/A	Voltage-to-Frequency Converter 100 kHz Max	0.01%

DIGITAL VOLTMETERS

PART NO.	RESOLUTION (BITS)	CONVERSION TIME	COMMENTS	ABSOLUTE ACCURACY (MAX)
ADD3501	3½-Digit	200ms	3½-Digit LED DVM	0.05%
ADD3701	3¾-Digit	400ms	3¾-Digit LED DVM	0.05%

What's new from the National Archives?

51 ☐ Data Acquisition Handbook ($7.00)*

F9 ☐ ADC0831, ADC0832, ADC0834, and ADC0838 A/D Converter Data Sheet

G0 ☐ ADC0833 A/D Converter Data Sheet

G1 ☐ ADC1001 and ADC1021 A/D Converter Data Sheet

57 ☐ DAC1280A and DAC1285A Data Sheets

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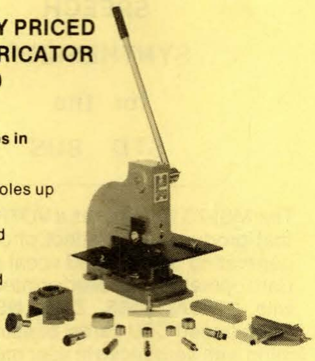

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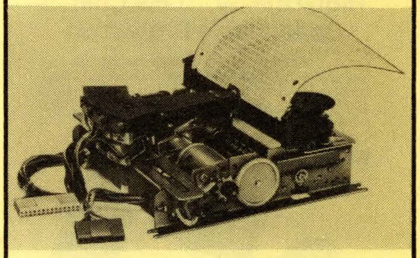

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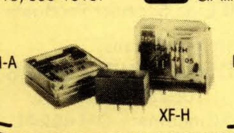

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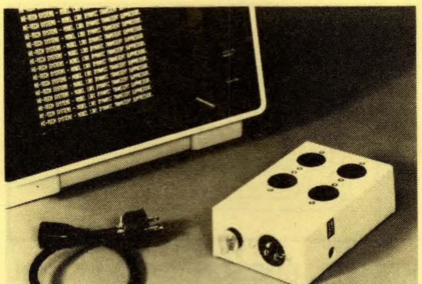

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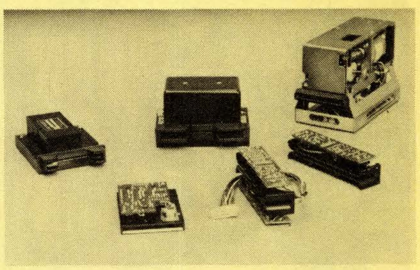

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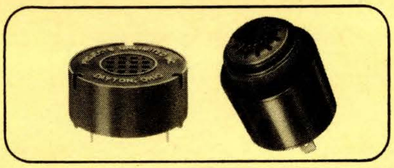

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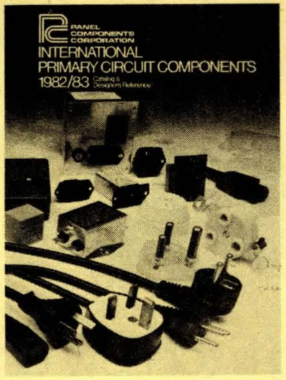

Panel Components Corporation International Primary Circuit Components 1982-83 Catalog and Designers Reference

New 1982-83 catalog and design reference contains detailed descriptions of primary circuit components with international and North American product safety approvals. Primary circuit connectors, RFI filters, international cords and cordsets, international plugs, sockets, and socket strips are covered. Each product section is preceded with a description of applicable international standards and requirements. Suggested guidelines for specifying each component type are also included.

Panel Components Corporation, P. O. Box 6626 Santa Rosa, CA 95406, (707) 523-0600

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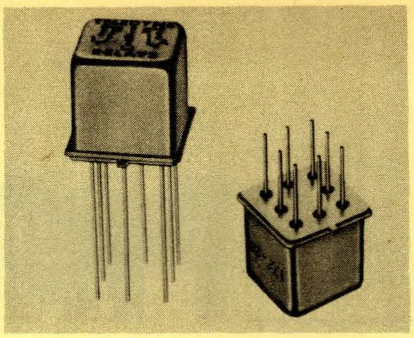

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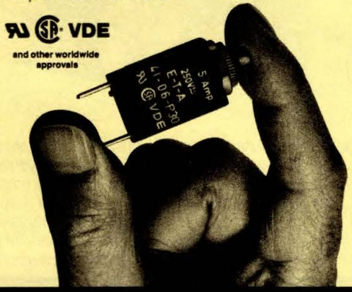

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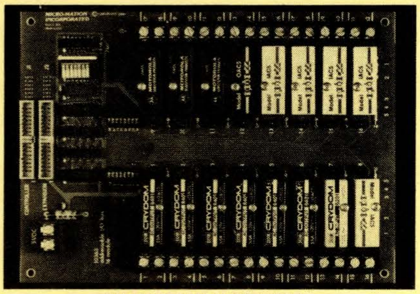

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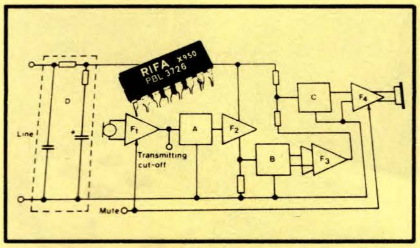

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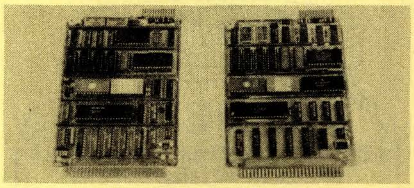

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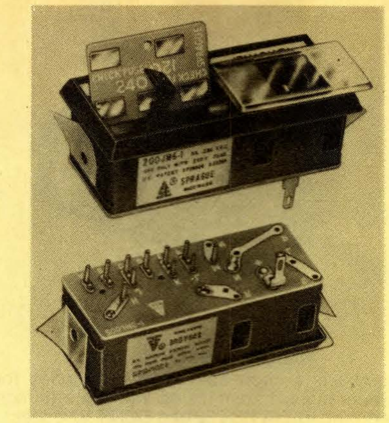

FUSED MULTI-VOLTAGE CONNECTORS.
Series 200JM6 devices for international equipment manufacturers operate with choice of 4 line voltages. Permit manufacturers to use single standard connector for equipment operating at 100, 115-120, 220, and 230-240 VAC, 48-440 Hz. Accept standard IEC Type V 3-pin plug. Designed with integral fuse holder and fuse pull. Write for Engineering Bulletin 8801. **Sprague Electric Co.**, 491 Marshall St., North Adams, Mass. 01247. 413/664-4411.

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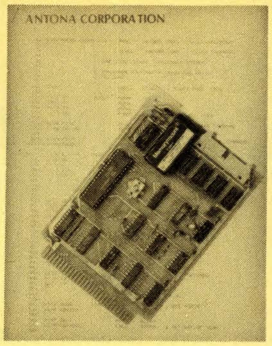

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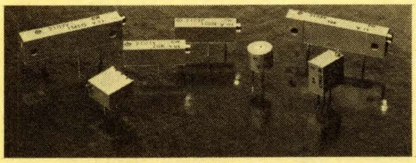

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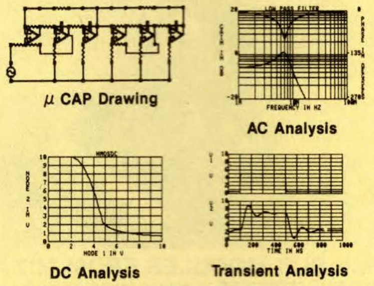
CIRCLE NO 157

μ CAP
CIRCUIT ANALYSIS SOFTWARE



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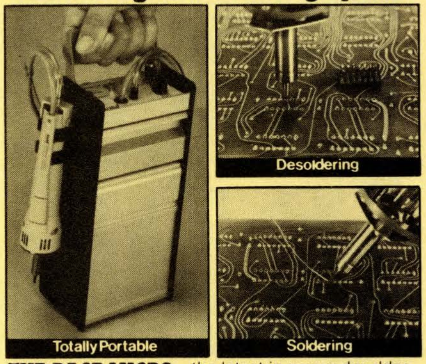
Finally...a portable power desoldering and soldering system.



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Tokyo 150 Japan. Telex: J28551

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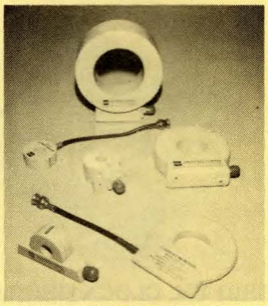

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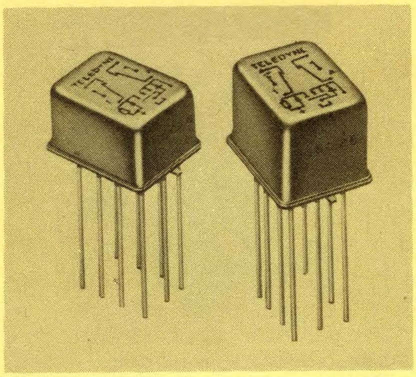

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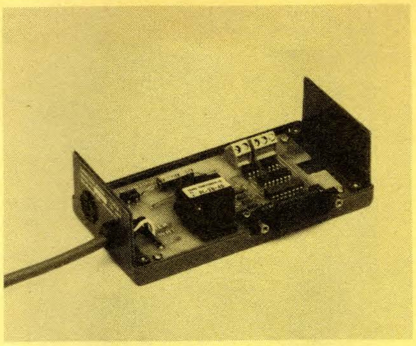

M-1 Short Haul Modem

The M-1 is a short haul modem intended for asynchronous transmission with an interface according to EIA RS-232 and CCITT V24 specs. M-1 can be used as a local communication link between computers, displays, printers, etc. Line driving is performed by two-way, balanced current loop. Transmission and receiving can occur simultaneously (full duplex). Pricing from $84.00. For data sheets and more information contact **Bo-Sherrel Company,** 6101 Jarvis Avenue, Newark, CA 94560 or phone 415-792-0354.

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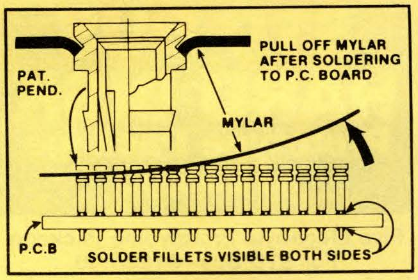

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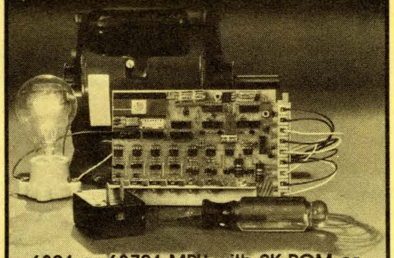

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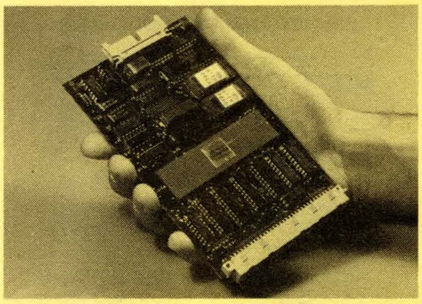

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VME8058 8 Slot Motherboard
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VME8400 Floppy Disk Cont.
VME8900 Debug Monitor

MIZAR INC. 2850 Bailey Road, Newport, MN 55055, (612) 459-2452

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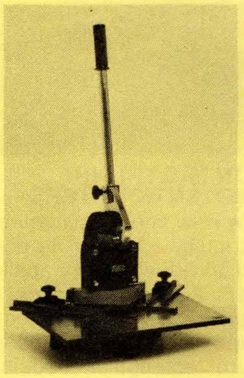

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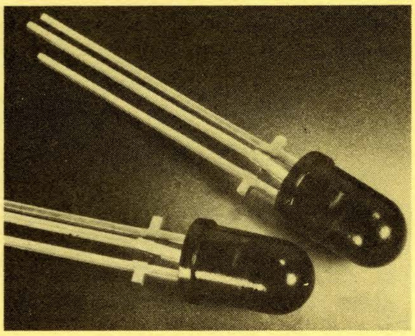

RED BLINKING LED

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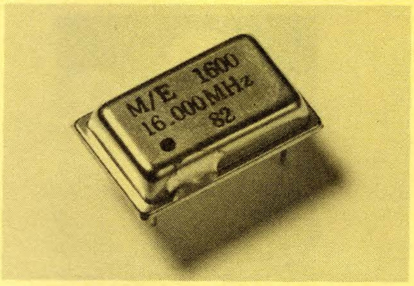

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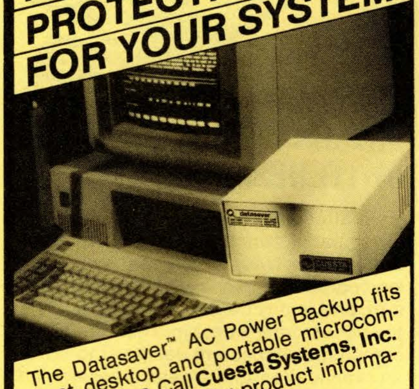

The Datasaver™ AC Power Backup fits most desktop and portable microcomputer systems. Call **Cuesta Systems, Inc.** at (805) 541-4160 for product information and application literature.

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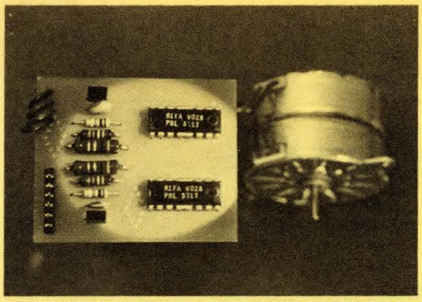

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PBL3717 is a bipolar integrated circuit intended to control and drive the current of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, and an output stage with built-in protection diodes. Two PBL3717's form a complete control and drive unit for two phase stepper motor systems.

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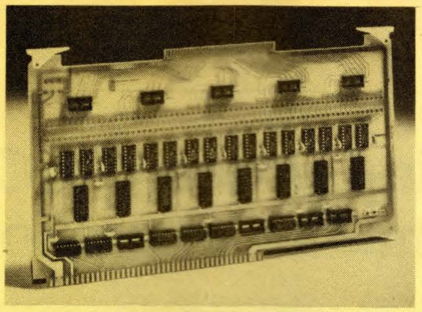

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SIM-64

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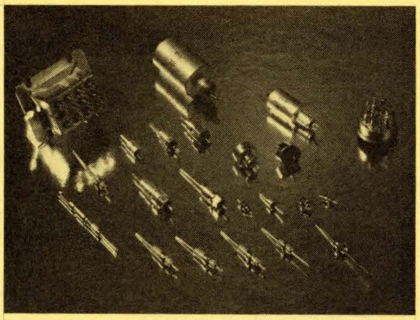

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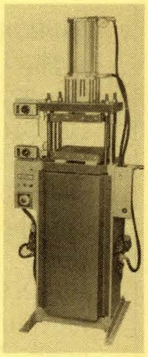

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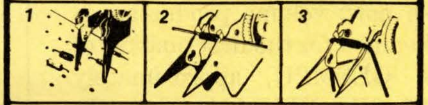

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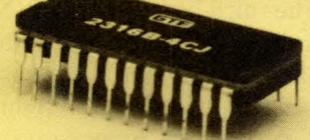

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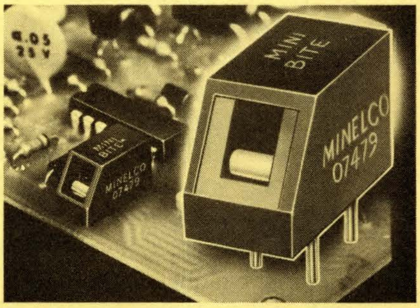

MINI PC FAULT INDICATOR New Minelco MINI-BITE™ (Built-in-Test Equip.) Indicator (#MB25) mounts on pc board, instantly locates a circuit fault at a glance, to minimize downtime. Dustproof internal drum rotates to highly visible contrasting color, latches to hold signal until reset. No filaments. Only .510" x .265" x .315" above board; gang-mount with ⅛" clearance. Ask for bulletin.

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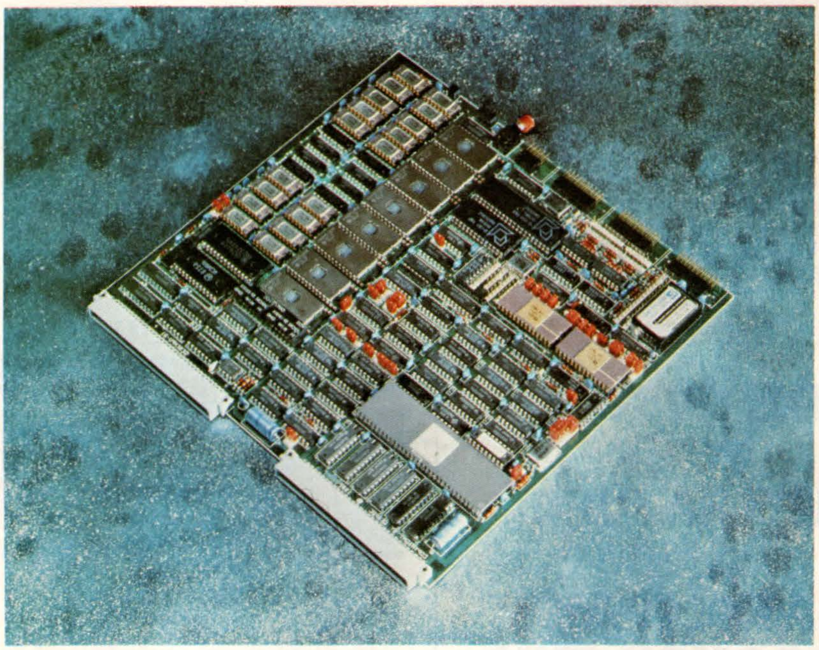
16/32-bit double-Eurocard μC modules support multimaster operation

Double-Eurocard-based G128 μC modules provide 16/32-bit multiprocessing power suited to high-performance industrial applications while maintaining compatibility with their manufacturer's single-Eurocard 8/16-bit G64 family. Three initial offerings—a 68000 CPU card, a ½M-byte memory option and a 4-channel serial communications controller—complement a currently available family of 60 single-Eurocard functions.



Based on double Eurocards, *modules in the G128 family support 16/32-bit multimaster operation. Three boards are available initially, including the 68000 processor card shown.*

Multimaster bus operation

The G128 backplane bus uses two 32-pin rows on each of two DIN 41612 connectors, keeping board-interconnection costs down. The boards' 220×233-mm double-Eurocard format features an extended 233-mm length that optimizes each card's functionality and reduces the need for bus transfers. In addition, all I/O is taken out, eliminating the need for dedicated rack slots. Fully compatible with the single-connector G64 bus, the G128 bus is a nonmultiplexed scheme with 32 data and 32 address lines that support as many as 16 processors in a multimaster design.

Three board functions provide the family's initial choices. The central - processor board, GESMPU-D1, uses the 68000 μP and includes 128k bytes of on-board memory (with parity control) to allow local execution of many key tasks without using the bus. In addition to the RAM, eight sockets accept as much as 64k bytes of EPROM, and two serial RS-232 or RS-422 interfaces accommodate synchronous or asynchronous communications. A timing controller (five 16-bit counters), interrupt-handling logic and a bus-arbitration controller that supports as many as 16 masters complete the facilities.

GESRAM - D1 system-memory board provides ½M bytes along with error-detection and -correction logic. It's organized as 256k words of 22 bits; six bits are utilized for correction of single errors and detection of multiple errors, including single bytes. All required refresh logic is included and can be used by several processor types.

The third board, the GESINT-D1, is a communications function designed for use as an intelligent interface. It reduces the load on the processor(s) by directly performing tasks such as protocol handling. Four asynchronous or synchronous channels compatible with RS-232 or -422 are available, along with four bidirectional 8-bit ports and five 16-bit counters. A dual-port μP utilizes eight memory sockets.

In development are two other processor options (16032 and 8086) and several other cards: a high-resolution color-graphics controller (640×480 window in a total display memory of 1024×1024 without interlace), a local-network controller that supports 50 stations over 300m of coaxial cable at communication rates to 800k bps, a hard-disk interface, and an analog I/O system.

Sample quantities are available now; volume production is scheduled for the first quarter of '83. GESMPU, approximately 5000 SF; GESRAM, 9000 SF; GESINT, 2500 SF.

Gespac SA, 3 Chemin des Aulx, CH-1228 Geneva/Plan-les - Ouates, Switzerland. Phone (022) 71 34 00.

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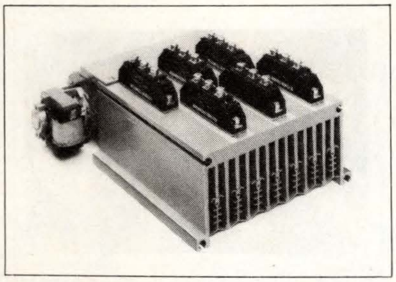

COOLING SYSTEM. For high-performance cooling of semiconductor modules, QLS 190 heat sinks with combined fan motor can be supplied with a milled mounting surface of 10-μm roughness. Available in three sizes with mounting surfaces measuring 190×100 to 191×200 mm, the system weighs 3.3 to 5.3 kg and uses a split-pole plain-bearing 220V/50-Hz motor with a running time of 30,000 hrs at the maximum environmental temperature of 40°C. 143 DM for a 191×100-mm - mount - area, silver-anodized, milled-surface piece with motor. **Austerlitz Electronic GmbH,** Postfach 1048, 8500 Nurnberg 1, West Germany. Phone (0911) 53 33 33.

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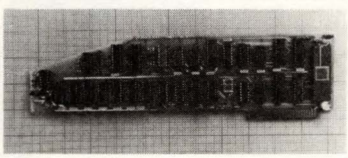

APPLE GRAPHICS. Adding the VGP peripheral card to Apple II computers provides a monochrome graphics capability of 512×512 pixels. An on-board vector-graphics processor draws lines and characters at rates to 1.5M pixels/sec, freeing the computer's processor for other tasks. Extra storage space and a more orderly memory map are provided by the card's integral 64k-byte memory—large sectors of address space no longer must be reserved in Hi-Res mode. You can store two pictures in memory and swap them instantly under software control; characters and lines may be mixed freely. £399. **Digisolve Ltd,** Cinder Lane, Castleford, West Yorks WF10 1LU, UK. Phone (0977) 513141.

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LOGIC ANALYZER. Expandable from 35 to 59 channels, the PM3551 combined logic-state and -timing analyzer makes extensive use of soft keys for instrument setup. All channels work in state-analysis mode to a maximum clock frequency of 15 MHz. You can configure eight of the channels for timing analysis to 50 MHz, and an optional extension provides 300-MHz analysis on four channels. Storage capacity equals 1k words, and selective-tracing mechanisms increase usefulness. Trigger facilities include multiple-word triggering and trigger on nonoccurrence of a sequence. **NV Philips' Gloeilampenfabrieken,** Science & Industry Div, Box 523, 5600 AM, Eindhoven, The Netherlands. Phone (040) 70 21 51.

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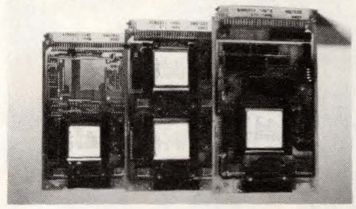

MEMORY CARDS. Three cards extend the choice of memory options in the 8-bit ECB family of μC modules. ECB-BM1 contains 128k bytes of nonvolatile bubble memory and costs 2700 DM; the larger 256k-byte ECB-BM2 version costs approximately 4600 DM. Both units work in conjunction with a controller card that accommodates a 1M-byte max capacity in 128k-byte steps. A 915-DM universal memory board, ECB-M, comes with a dc/dc converter and eight 24-pin sockets capable of housing RAM, ROM, PROM and EEPROM. On-board battery backup also allows use of CMOS RAM. All three cards come in standard 100×160-mm single-Eurocard format. **Kontron Microcomputer GmbH,** Breslauer Str 2, D-8057 Eching, West Germany. Phone (089) 3 19 01 1.

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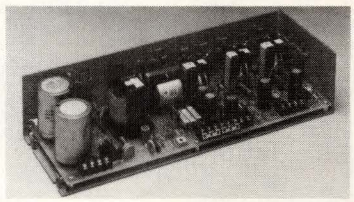

POWER SUPPLIES. Two additions to the Econoflex Series of open-frame power supplies provide four output rails. Both units produce 5V at 20A, 12 or 15V at 3.5 or 3A and −12 or −15V at 3.5 or 3A. The fourth output of Model EXQ180 is 24V at 2A; EXQ180/426 provides an extra 5V/1A rail. The supplies are designed to meet UL and CSA specs, and all are burned-in for 48 hrs at full load. Overvoltage protection on the main output rail is optional. Input voltage can be 95 to 132V or 190 to 264V; total output power equals 180W. Output variation is <0.2% for a ±10% line-voltage change and 50 to 100% change in load, and rms ripple equals 0.2% max. £140. Delivery, stock to 6 wks ARO. **Gould Power Supplies UK,** Raynham Rd, Bishop's Stortford, Herts CM23 5PF, UK. Phone (0279) 55155.

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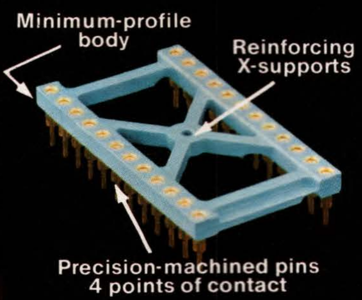

Available in 6 through 64 positions, Ansley Electronics DIP Sockets offer precision screw-machined pins for high integrity, high reliability contact. Plus a minimum-profile body to maximize air flow and space between boards.

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The byword is commitment. Look to Ansley Electronics as the complete across-the-board supplier for all your electronic interconnection needs. For data on our new DIP Sockets, adaptor plug assemblies, terminal carriers and socket pins, write today. Thomas & Betts Corporation, Ansley Electronics Division, 920 Route 202, Raritan, N.J. 08869. Or phone Customer Service at (201) 469-4000.

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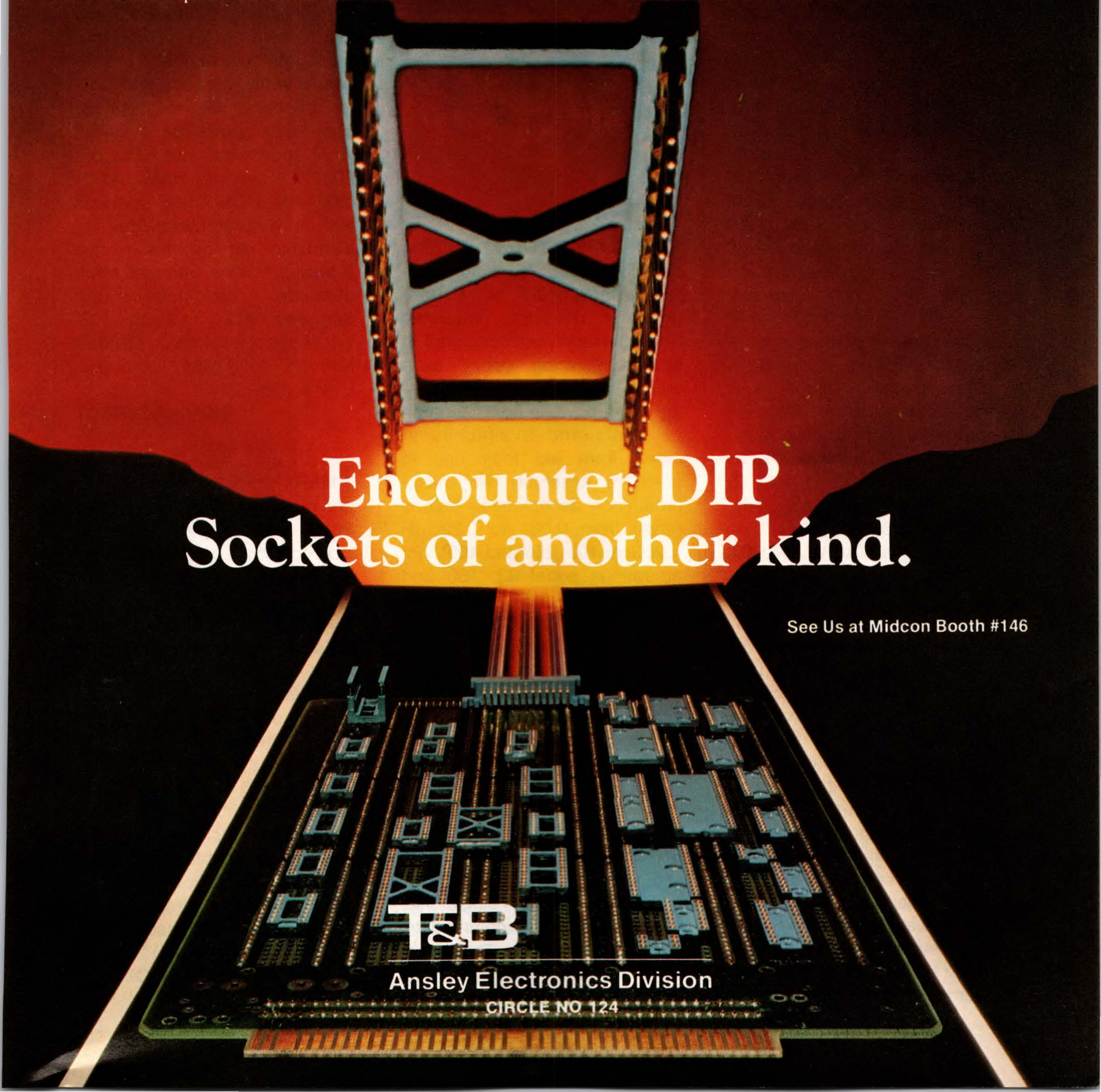

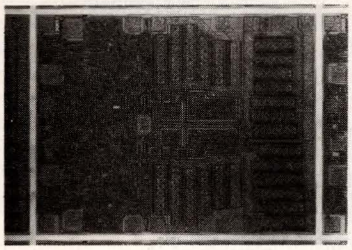

220W MOTOR DRIVER. Model L295 2-channel switch-mode driver IC accommodates inductive loads such as solenoids and stepping motors, providing effective power to 220W. Each channel is controlled by a TTL-compatible input and handles repetitive peak output currents of 2.5A at supply voltages to 46V. Load current is externally programmable, and the circuit is internally protected against overtemperature conditions. Switch-mode operation permits driving two solenoids; two L295s may be used together to drive the four phases of a unipolar stepping motor or a bipolar stepping motor in a bridge configuration. Samples now available in 15-lead Multiwatt plastic packages. **SGS Ates SpA,** Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551.

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TRAVELING-WAVE TUBES. Modular TWTA traveling-wave-tube amplifiers are designed for use in 140M-bps digital microwave radio links and comprise a high-linearity traveling wave tube, a power supply and an optional matched control unit that indicates status. The tubes have a third-order intercept point of 50 dBm min and a double-depressed collector for increased efficiency, suiting them for microwave digital and SSB radios. Available in 4-, 6- and 11-GHz bands with linear output power to 10W, the tubes can be driven by a supply that operates from any voltage between 24 and 60V dc. For satellite earth stations in the 14-GHz range, tubes are available with 300 and 750W output power, with a permanent-magnet system integrated. **Siemens AG,** Postfach 103, Wittlesbacherplatz 2, D-8000 Munich 1, West Germany. Phone (089) 234 1.

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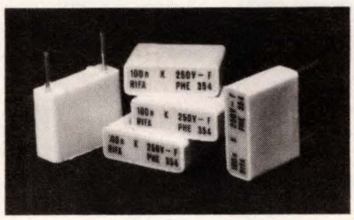

FILM CAPACITORS. PHE354 miniature metallized film capacitors incorporate a wound-polyester dielectric metallized with aluminum, encapsulated in self-extinguishing epoxy resin and housed in a self-extinguishing polypropylene box. Stand-off terminals and availability in taped form aid their use in pc-board assembly via mass-production techniques. Values range from 0.001 to 0.22 μF ±20% at 100, 250 and 400V dc; ac ratings equal 63, 160 and 200V. The components operate over −40 to +100°C. ESR is specified at high frequencies, and construction features optional lead spacings of 5, 7.6 or 10.2 mm. **RIFA AB,** Box 2, S-163-00 Spånga-Stockholm, Sweden. Phone (08) 752 25 00.

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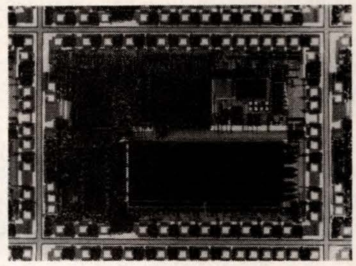
ENTERTAINMENT μCs. For TV and video-equipment use, two additions to the SDA single-chip NMOS μC family accommodate low-end applications. These versions of the 8021 μC are capable of digital frequency



synthesis, VCR tape-run control and station search. Housed in 28-pin packages, the 2020 and 2030 retain an 8-bit CPU, four analog outputs with 6-bit resolution, a serial interface and logic for decoding infrared signals. The 2020 sports 64 bytes of RAM and 1k bytes of ROM; the 2030, 64 bytes of RAM and 2k bytes of ROM. Both devices feature 10-μsec cycle time; the instruction set includes 1- and 2-cycle functions. Samples available now. Approximately 9 DM. **Siemens AG,** Postfach 103, Wittlesbacherplatz 2, D-8000 Munich 1, West Germany. Phone (089) 234 1.

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TIMER. Operating from 5V dc and drawing <300 mA, the Solid State Elapsed Time Indicator incorporates a crystal-controlled clock and offers a choice of four counting ranges: 9999 or 999.9 hrs or sec, 9 min 59.9 secs, or 9 hrs 59.9 min. It can be used in either mains- or battery-operated equipment and incorporates a memory. The unit fits into a standard 92×45-mm DIN panel cutout; overall size equals 96×48×74.6 mm. The four LED digits are 14 mm high, and four output connections are provided for power, enable and reset. £45. Delivery, 2 to 3 wks ARO. **Startronic Ltd,** Beeching Rd, Bexhill on Sea, Sussex TN39 3LG, UK. Phone (0424) 214291.

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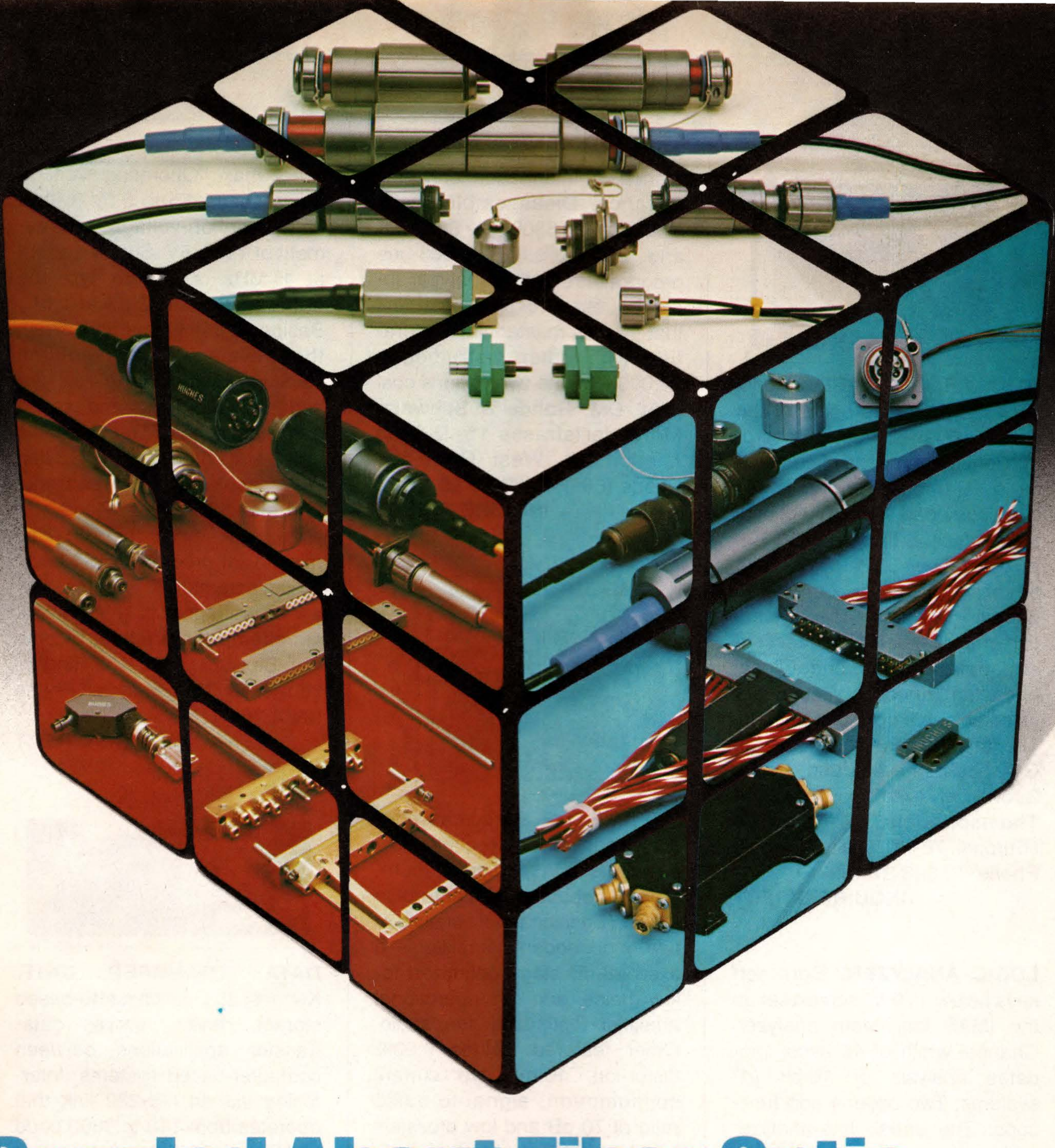

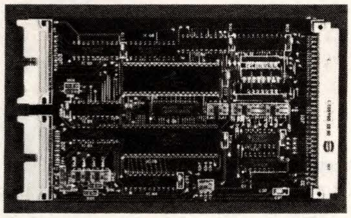

PARALLEL-I/O CARD. Model EFS-PIA 2A offers users of the single 100×160-mm Eurocard-bus family the means of connecting a μP through 32 parallel I/O lines equipped with bidirectional buffers (with a TTL fanout of 10). It uses two 6821 PIAs with several software-controlled operating modes. The system can employ four 8-bit bidirectional ports and eight control lines; operating direction is jumper selectable in blocks of eight bits. The family is based on the 64-pin G64 backplane bus and uses a 2-row DIN 41612 connector. **Thomson-Efcis,** 45 Avenue de l'Europe, 78140 Velizy, France. Phone (3) 946 97 19.

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LOGIC ANALYZER. Eight soft keys below its 9-in. screen set up the IMAS logic-state analyzer. Channel width of 48 accommodates analysis of 16-bit μP systems. Two options add functions: The serial data-analyzer probe and generator aids in checkout of bidirectional RS-232 and current-loop interfaces, and a counter/signature-analyzer add-on allows program testing by determining the frequency of data words (event counting) and the time spacing of equal and different digital events (time-difference measurement). A second signature-analysis function works to 40 MHz. IMAS features 12.5-MHz clock frequency, memory depth of 250 words, 16 trigger levels with qualifier and several clock inputs, and selective tracing—on program-branching information only, for instance. Disassemblers are available for 6800/2/9, 8080/5/6 and Z80 μPs. IEEE-488-bus programmable, the analyzer incorporates a bidirectional link that permits master/slave operation with other instruments. 24,000 DM; the two options cost 5250 DM. **Rohde & Schwarz,** Mühledorfstrasse 15, D-8000 Munich 80, West Germany. Phone (089) 41 29 26 25.

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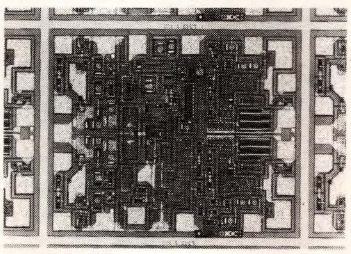

PREAMP. For stereo-cassette-player applications requiring low noise, the TDA3420 dual preamplifier IC specs total input noise <1 μV. Each channel consists of two independent amplifiers—a fixed 28-dB stage optimized for low noise and an operational amplifier optimized for audio. Other features include 0.03% distortion, 10-mA typ current consumption, signal-to-noise ratio of 70 dB and low crosstalk (obtained through physically separate ground and supply lines for each channel). Operating from one 8 to 20V supply, the device comes in a 16-pin DIP or Micropackage. A similar circuit, TDA3410, serves autoreverse tape applications. **SGS-Ates SpA,** Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551.

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4k CMOS RAM. Model PCD5114 1024×4 static CMOS RAM specs access time of 200 nsec max. Operating voltage range spans 4.5 to 5.5V, with a data-retention-voltage requirement of 1 to 5.5V. Supply current at 1 MHz is 10 mA typ; the standby value is 2 μA at 1.5V. Besides a 64×64 memory array, the device includes column selection, column and row decoders, write logic and sense amplifiers. It has TTL-compatible and 3-state data I/O. The $\overline{CE}$ and R/$\overline{W}$ inputs control read/write and standby modes. Read and write cycle times equal 200 nsec min. Initial production will be in 18-pin ceramic DIPs, followed by a version in plastic. **N V Philips' Gloeilampenfabrieken,** Elcoma Div, Box 523, 5600 AM, Eindhoven, The Netherlands. Phone (040) 79 11 11.

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DATA - TRANSFER UNIT. Konnect 2, a minicassette-based storage device, serves data-transfer applications between computer-based systems. Interfacing via an RS-232 link that operates from 110 to 9600 baud or via an 8-bit parallel port, it specs storage capacity of 64,000 characters on each side. Error rate of the digital cassette mechanism is less than 1 in 10^8. Powered from 220 to 240V ac, the device comes in a 220×230×105-mm plastic case. A built-in μP system allows a range of code-conversion options, including EBCDIC, TTS, reverse TTS and ASCII. £950. **Interset Computer Systems Ltd,** New Rock, Chilcompton, Bath, Avon BA3 4JE, UK. Phone (0761) 232606.

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CIRCLE NO 126

A Question of Law

Edited by Jesse Victor

Knowing applicable federal and state laws can help prevent warranty disputes

L J Kutten, Attorney at Law
St Louis, MO

Written warranties can provide important protection against defective electronic equipment. If you buy a malfunctioning switching power supply or microcomputer, a warranty can ensure that the product's manufacturer and/or seller will fix or replace the faulty merchandise.

However, the manufacturer/seller's view of a warranty is completely different from yours. The former hopes to limit its liability for defective equipment while at the same time giving express statements and promises that will keep you satisfied. You, on the other hand, see a warranty as your sole defense against shoddy or defective merchandise.

Furthermore, warranties for commercial products can come under different warranty-control laws than do those that apply to consumer transactions. And the many state statutes that limit and modify warranty regulations complicate the situation.

Thus, to understand precisely what protection a warranty affords, you must have a basic knowledge of the relevant federal law and how state statutes can modify a warranty's provisions.

Until 1975, Article 2 of the Uniform Commercial Code (UCC) functioned as the basic warranty-control model code, governing both commercial and consumer transactions. An attempt by the legal community to formulate a consistent body of law relating to commercial-product sales, the code contains provisions dealing with the creation of express and implied warranties and limitations to the protection they afford.

In 1975, however, Congress passed the Magnunson-Moss Warranty Act (15 USC 2301, *et seq*). Applying to consumer transactions and not to commercial transactions between businesses, Magnunson-Moss significantly altered pre-1975 law by setting standards for consumer warranties.

This article thus examines UCC-created express and implied warranties and how they can be disclaimed. It also considers state modifications to the UCC and the Magnunson-Moss Warranty Act.

Software a special case under the UCC

The Uniform Commercial Code's Article 2 applies only to "goods," not "services." UCC Section 2-105 defines "goods" as "all things (including specially manufactured goods) which are movable at the time of identification to the contract for sale other than the money in which the price is to be paid." Formidable legalese notwithstanding, all computer and electronics hardware clearly falls under this definition. Computer software, however, is a somewhat special case; whether it's to be considered "goods" has not been finally decided by the courts.

In the early days of the computer industry, software was not considered goods because its implementation usually included modification to fit each user's needs. The proliferation of turnkey systems, though, is changing the legal situation. In 1978, for example, a federal district court dealing with a turnkey computer system ruled that software could be classified as goods.

Packaged software, then, will increasingly be defined as goods under the law. Thus, if software is sold off the shelf without the expectation of modification, it can be considered goods and come under the UCC. If, on the other hand, it must be specially written or modified for a particular end user, it will be considered a service and not fall under the UCC's warranty provisions.

Creating express warranties

The UCC defines two kinds of warranties: express and implied. Express warranties are created in three ways. In the first type of express warranty, if a seller makes any factual statement or promise to a buyer relating to an electronic product, the equipment must function as described. Thus, if a manufacturer claims its electronic equipment will work from 110 or 220V without switching, it must do so or else violate an express warranty. Furthermore, if a seller provides a written description of its product, the equipment must conform to that description. For example, if you order RAM chips that are described as 16k devices, the seller cannot deliver 4k devices without violating an express warranty.

Finally, any sample or model made part of a business transaction creates the express warranty that the goods shall conform to the sample or model. Therefore, buying 1000 CMOS RAM chips based on a sample of 10 and finding that the other 990 are not the same quality as the sampled parts violates an express warranty.

In addition to express warranties, the UCC creates two types of implied warranties: fitness for a particular purpose and merchantability.

The merchantability provision states that all goods sold by a merchant must be of the type described and reasonably fit for the general purpose for which they are sold. If you buy a triple-output power supply that continuously breaks down and the unit remains inoperable after numerous service calls, the seller has violated an implied merchantability warranty.

Fitness for a particular purpose applies when a seller has reason to know the particular purpose for which a product is required and the buyer relies on the seller's skill or judgment to furnish a suitable product. This implied warranty is violated, for example, when a supplier recommends a power-supply system based on a user's power needs and the unit does not in reality fulfill those needs.

Of the two types of implied warranties, the warranty for a particular purpose can provide the most protection for a buyer of electronic products: It's very difficult for a product's supplier to deny knowledge of participation in the installation of the buyer's system through recommending equipment, performing design work or furnishing software.

Disclaimers can limit warranty protection

Many sellers prepare sales agreements and contracts that limit or disclaim their warranty liability, and such a disclaimer can sharply limit a buyer's protection against faulty electronic equipment. Under the UCC, a disclaimer of the implied warranties of merchantability and fitness must be "conspicuous" and must be in writing. Furthermore, a disclaimer of the merchantability warranty must mention "merchantability." (An alternative way to disclaim implied warranties is to sell a product using conspicuous phrases such as "as is," or "with all faults," although this approach is seldom used for obvious reasons.)

The UCC's "conspicuous" requirement is difficult to define accurately; numerous court cases have attempted to pin down this term. Generally, though, if a disclaimer appears in capital letters in a contrasting typeface to the other faces surrounding it and the disclaimer on the whole is in larger type than the rest of the agreement, the disclaimer is conspicuous. However, if the disclaimer is indistinguishable from the rest of the contract, it's not considered conspicuous.

Confirmed prior knowledge of a disclaimer provision by a buyer before the purchase of an electronic product is not required under the UCC—nor is notice of the disclaimer provision. The buyer is presumed to have read, understood and assented to everything he signs.

Thus, if a disclaimer is printed on the last page of a 10-page sales order and if it fulfills the UCC's conspicuousness requirement, a buyer is presumed to have read and agreed to it even if he did not in fact see it. Note, though, that warranties cannot be disclaimed *after* a sale: A disclaimer that first appears in a manual delivered after a sale is void.

Ad claims cannot be disclaimed

Not all warranties can be disclaimed, however. A seller, for example, can't disclaim any express warranties made in its advertising material. If an ad says a product will perform a certain function, that claim cannot be disclaimed.

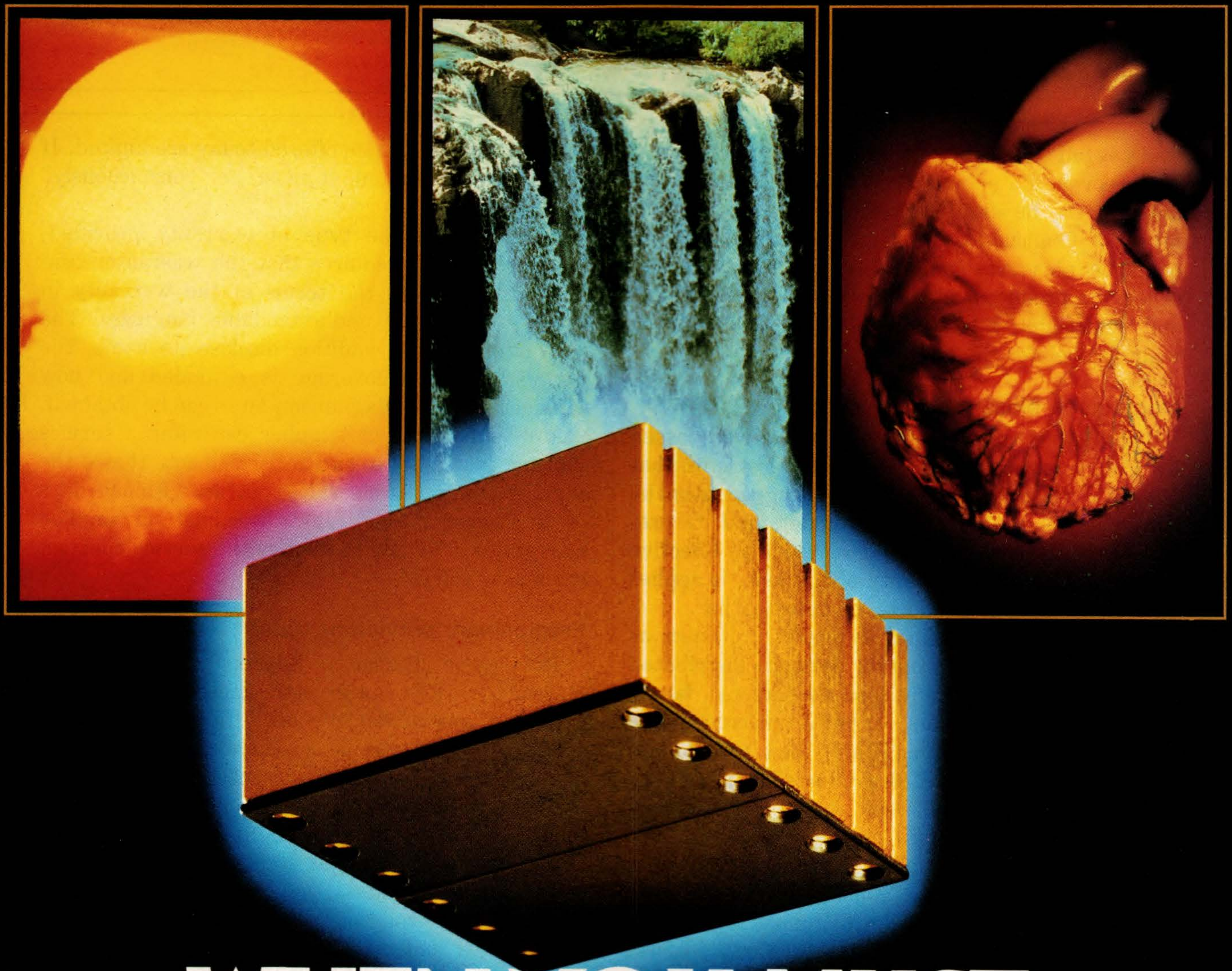
For example, if you buy a ac/dc converter advertised as putting out exactly 10 to 100V dc in 10V steps and after buying it you discover it delivers 10.9 to 100.9V, and if you did not know of this problem before purchase, any disclaimer relating to the problem is ineffective. Realize, too, that with regard to personal injury, no disclaimer is worth the paper it's printed on.

A "failure of consideration" can also set limits on warranty disclaimers: A disclaimer thus cannot excuse the failure to supply the goods forming the basis of a business transaction. For example, a checkbook-maintenance program must function as a checkbook-maintenance program. If it is delivered so riddled with bugs that it won't operate, the seller has not delivered what was bargained for, no contract exists, and the buyer is entitled to a refund of the purchase price on the theory that the seller never delivered the product.

State statutes modify UCC provisions

Several states have modified the UCC's provisions on disclaimers. Maine and Massachusetts state laws, for example, assert that warranty disclaimers cannot apply to the sale of consumer goods or services.

California has the most extensive consumer warranty law. This Song-Beverly Consumer Warranty Act urges every manufacturer of consumer goods sold in the state with express warranties to maintain sufficient service and repair facilities, in the state, to carry out its warranties. If a manufacturer does not maintain "sufficient facilities," it becomes liable to



every retail seller of its consumer goods.

Moreover, if a manufacturer willfully violates the law and the buyer of a product suffers a physical injury or financial loss, the buyer can receive triple damages plus reasonable attorney fees. A retail seller of a product is also entitled to triple damages and reasonable attorney fees if a manufacturer willfully violates the statute.

Magnunson-Moss regulates consumer products

The Magnunson-Moss Warranty Act was passed by Congress to solve some of the problems that allegedly arose under the UCC. Designed to make consumer warranties easier to understand, to prevent deceptive practices and to provide an effective means of enforcing warranty obligations, it applies only to "consumer" products, as noted earlier.

Magnunson-Moss defines a consumer product as any tangible personal property normally distributed in commerce and normally used for personal, family or household use. Thus, a home microcomputer would fall under the act; an IBM System/1 would not.

However, some electronic products fall into a gray area of the law. For example, a product designed primarily for business use (eg, a CMOS chip) but available for sale to consumers (eg, at any electronics hobby store) might be considered a consumer product and thus come under Magnunson-Moss, if it costs the buyer more than $5. If ABC Co, therefore, displays its business microcomputers in a showroom open to the public and will sell and install its product in an individual's home, it is considered to sell a *consumer* product, even though more than 75% of its sales are to businesses.

(Note that under Magnunson-Moss, a supplier is defined as any person engaged in the business of making a consumer product directly or indirectly available to consumers. Thus, it could be the product's manufacturer, wholesaler or retailer.)

Defining full and limited warranties

There is no requirement in Magnunson-Moss that a supplier provide a warranty, but if it does, the warranty can be full or limited.

Under a full warranty, the warrantor must repair or replace any defective or malfunctioning product within a "reasonable time" and without charge. If the supplier cannot fix the product after a "reasonable number of attempts," the buyer must get a cash refund or a replacement of the product without charge. If the product's failure, however, is attributable to unreasonable use—including improper maintenance—the supplier is not liable under the law.

Under a limited warranty, the warrantor can limit its responsibilities to repair and replace defective goods; most warranties offered today are limited. If a warranty is limited, it must be "conspicuously" labeled as such.

Regardless of the type of warranty provided, Magnunson-Moss requires that the warrantor conspicuously disclose the terms of the warranty in simple and readily understandable language. The warrantor must in addition disclose its name, the parties to whom coverage is extended and how satisfaction under Magnunson-Moss can be obtained.

A manufacturer or supplier can offer a service contract instead of a warranty. But note that if the supplier enters into a service contract within 90 days of a product's sale, any disclaimer of implied warranties is invalid so long as the service contract remains in effect.

Enforcement provisions differ

The major difference between the UCC and Magnunson-Moss concerns the methods of enforcement available under the law. Under the UCC, a buyer of an electronic product must prove the manufacturer provided a warranty under the UCC, that the product failed to live up to it, that the buyer's loss was caused by the product's defect and that he suffered damages as a result. In contrast, under Magnunson-Moss, you can sue a warrantor in federal or state court if it has been given reasonable opportunity and failed to cure a breach of its warranty or service contract. A court, in addition, can include court costs and attorney's fees as part of any settlement; under UCC law suits, court costs and attorney's fees are not usually allowed.

In sum, if you are involved in any stage of an electronic product's design, or if you buy electronic products from other manufacturers, keep the following warranty-related considerations in mind.

- Under the provisions of the Uniform Commercial Code, an electronic product must function as described in a factual statement or promise made by its seller, must conform to the seller's written description and must conform to a sample or model contained in a business transaction. If it does not, an express warranty is violated.
- Packaged, commercially available software will be increasingly considered as "goods" by the courts and thus fall under the UCC's warranty provisions. Note that any disclaimer of implied warranty contained only in a software package and not visible to a buyer before a sale might not be considered valid under the law.
- Understand the UCC's implied-warranty provisions and take care that your product does not violate the merchantability or fitness-for-a-particular-purpose provisions. Be especially careful

A Question of Law

about not violating the latter type of warranty.

- Keep in mind the UCC's disclaimer provisions and how they might be modified by particular state laws. If you sell an electronic product, make sure any disclaimer of implied warranty fulfills the UCC's conspicuousness requirement. If you buy electronic equipment, study any disclaimers carefully before the transaction is completed.
- Make sure that any consumer electronic product you sell does not violate Magnunson-Moss warranty provisions. Realize, though, that the proliferation of microcomputers into home applications, the use of "personal" computers in offices and the rise of videotex and teletext systems is creating a gray area in defining consumer versus commercial products that will need clarification by the courts. **EDN**

L J Kutten, JD, received the Juris Doctor degree from Washington University (St Louis, MO). A member of the Missouri and Illinois Bar Associations, he is currently in private practice specializing in all aspects of law relating to microcomputers. Kutten is the author of *Consumer Protection for the Microcomputer Owner,* a booklet for μC users.

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NEXT TIME

EDN's December 17 issue is our 16th semiannual Product Showcase, an invaluable compendium of information on the most noteworthy new-product introductions of the past 6 months. You won't want to be without this fact-filled reference issue, which is organized into seven key product areas:

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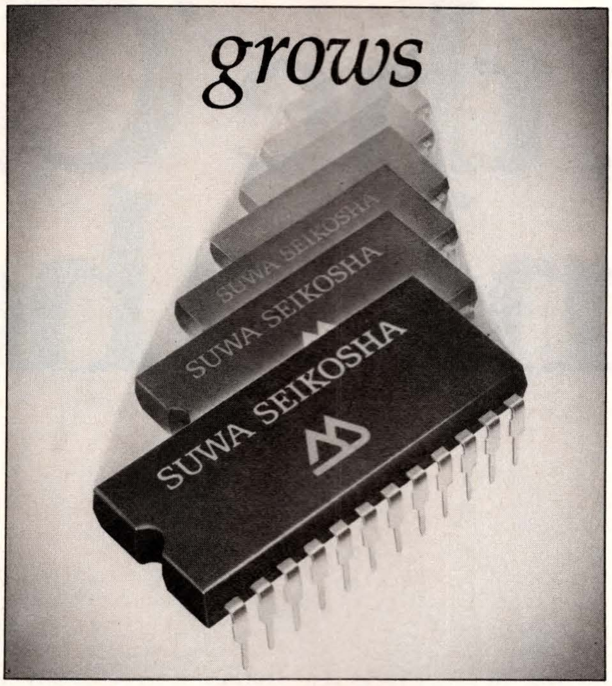

Suwa Seikosha, a major manufacturer of the famous SEIKO watches, is now producing new Static RAMs, Mask ROMS, Microcomputers, Voice Synthesizers and a host of other new products not yet released. As a pioneer of quartz watch technology, the company consistently developed and manufactured its own miniature electronic parts and IC's. Now a recognized specialist in the broad field of CMOS LSI, Suwa Seikosha is working aggressively to extend its position as a major-source supplier of Microcomputer Chips, Memories, Time Standard ICs, Voice Synthesizers, LCD Drivers, CMOS LSIs for Watches and Clocks, and Custom LSIs. OEMs are invited to contact Suwa Seikosha regarding new or existing products in these fields. Furthermore, inquiries are solicited regarding requirements in other fields that might benefit from Suwa Seikosha's most-advanced CMOS LSI technology. *Suwa Seikosha is a* growing *specialist in CMOS LSI.*

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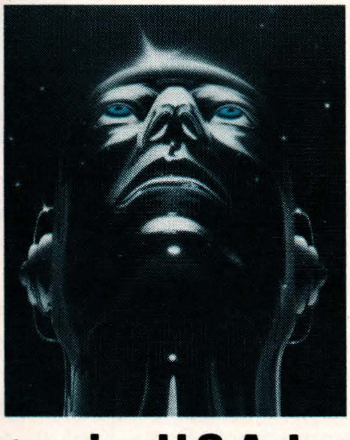

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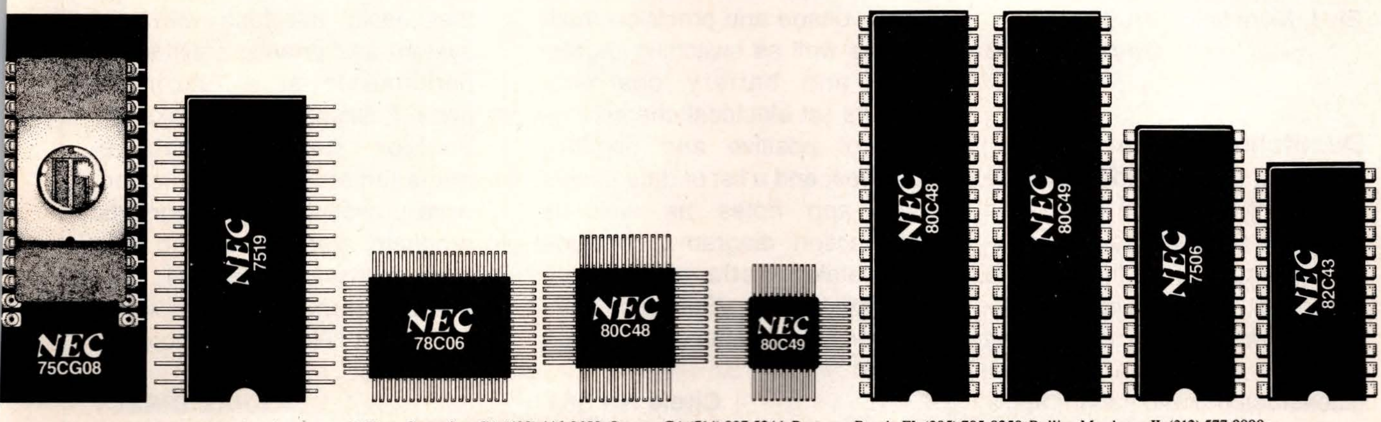

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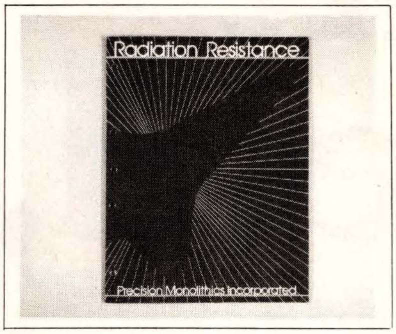


Resisting radiation

Highlighting a line of standard linear ICs found to exhibit a consistent resistance to radiation, this 4-pg brochure lists results from device testing at various total-dose levels, illustrated in graphs. A diagram shows a typical npn transistor, illustrating the location and characteristics of its silicon-nitride passivation layer. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.

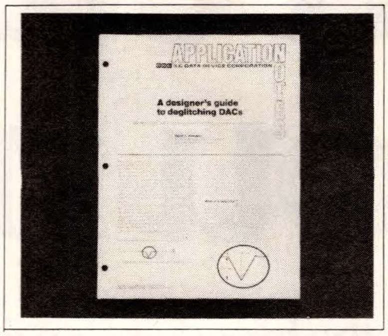
Circle No 378

Data details 2400-bps modems

With product specs, application diagrams, functional charts and panel callouts, this brochure describes MX Series 2400-bps modems. It highlights the five models' capabilities for both domestic and international operation, including multipoint, point-to-point, leased- or dial-up-line and network-control applications. **Codex Corp,** 20 Cabot Blvd, Mansfield, MA 02048.

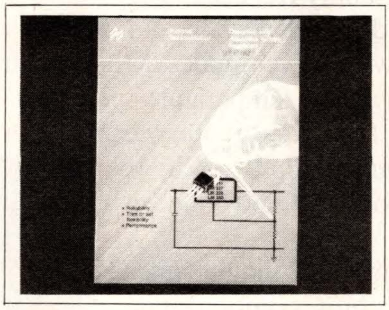
Circle No 379

Deglitching DACs



This 4-pg app note identifies the causes of glitches in DACs and presents solutions to the problem. It describes the function of a deglitcher and provides guidelines for selecting one. A timing diagram details a DAC/deglitcher/latch combination; application hints for layout, noise reduction and use of latches, plus photos and specs, complete the booklet. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 380



Design with adjustable voltage regulators

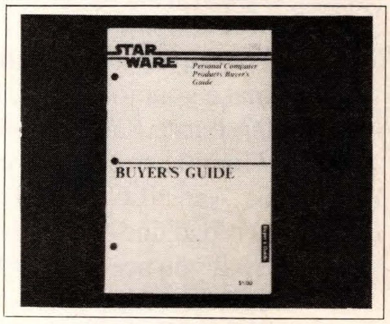
Beginning with a brief history of voltage regulators, this 18-pg pamphlet discusses unit performance factors such as line, load and thermal regulation. It also points out the advantages of using adjustable regulators: acceptance of high input voltages and improved current limiting. Diagrams illustrate basic regulator circuits and high-current, high-voltage and precision models as well as switching regulators and battery chargers. Charts list electrical characteristics of positive and negative devices, and a list of data sheets and app notes as well as connection diagrams conclude the catalog. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Circle No 381

MOS/LSI data

This 400-pg 1982 catalog features a line of MOS LSI and VLSI devices. Divided into separate sections covering data communications, CRT displays, floppy-disk controllers, printers, baud-rate generators, keyboard encoders and μP peripherals, it describes function, usage specifications and essential parameters for each product. Charts, circuit diagrams, graphs, flowcharts and photographs illustrate the book. The manufacturer's quality-control programs are discussed, and a cross-reference index and a list of company representatives and distributors conclude the catalog. **Standard Microsystems,** 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100.

Circle No 382



Hardware and software for the IBM PC

A *Buyer's Guide* for the IBM Personal Computer, this 28-pg catalog describes and gives prices for hundreds of products that easily interface with that system and provide satisfactory performance at a reasonable price. Published every 6 wks, the booklet details database-management, data-acquisition, word-processing and diagnostic products, plus games and software. Single copies, $1; 1-yr subscription, $8. **Starware,** 1701 K St NW, Washington, DC 20006.

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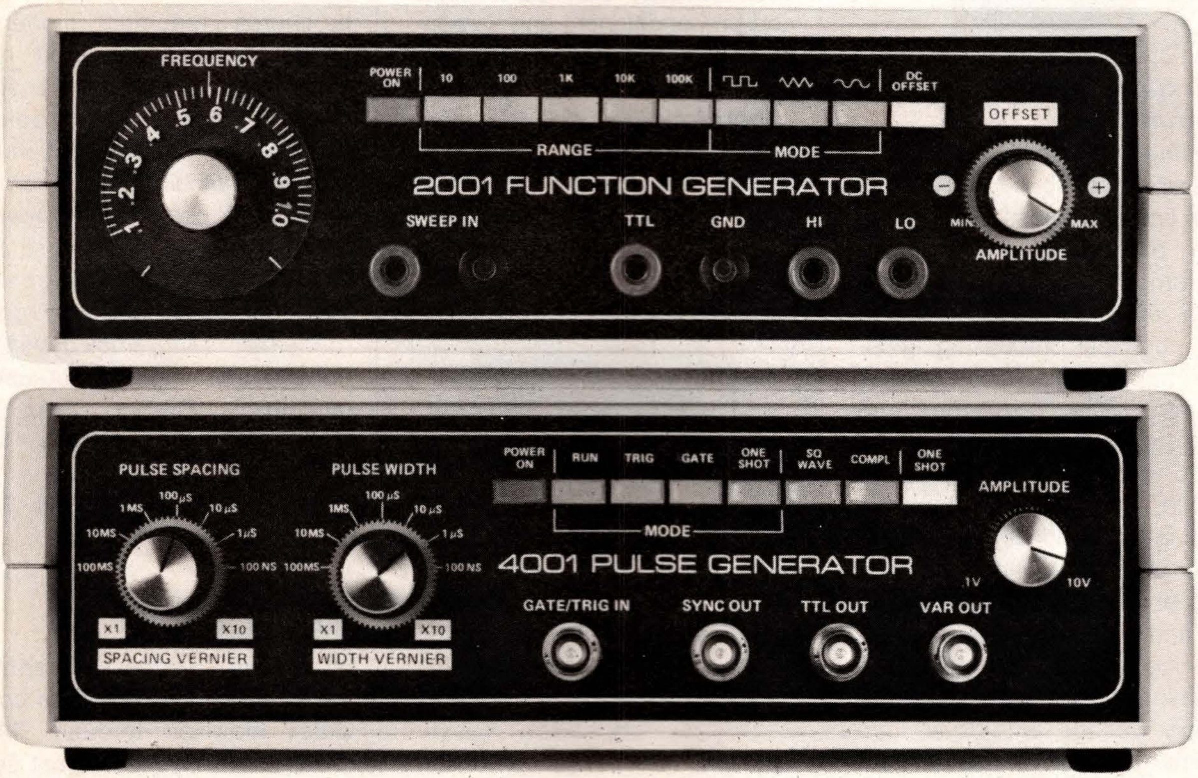

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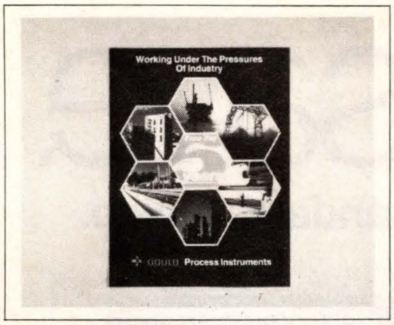
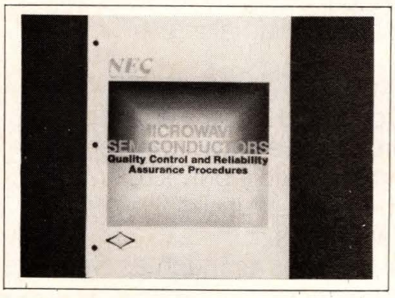


Using process instruments

Working Under the Pressures of Industry describes applications for a line of process instruments and their use in offshore platforms, nuclear power stations, pulp and paper processing, chemical processing, pipeline applications and general industry. The 12-pg brochure also details the company's "free for 5-yr" warranty. Specs for P3000 Series transmitters, including magnetically controlled zero and span, noninteracting zero and span, ±0.25% accuracy and corrosion-resistant SS housing and wetted parts are examined. A graph compares supply voltage with total loop resistance, and photos accompany product tables. **Gould Inc,** 1280 E Big Beaver Rd, Troy, MI 48084.

Circle No 383



Controlling semiconductor quality

Microwave Semiconductor Quality Control and Reliability Assurance Procedures details quality standards for a line of semiconductors. The 14-pg brochure contains specs and flow diagrams for bipolar transistors, GaAs FETs, IMPATT diodes and passive diodes; schematics include the new CX military-grade JANTX-equivalent parts. Tables outline assurance standards, examinations, drift parameters and preconditioning and screening tests for the microwave devices. **California Eastern Laboratories Inc,** 3005 Democracy Way, Santa Clara, CA 95050.

Circle No 384

Wire-wrapping techniques

Catalog 82-36P features tools and equipment for telecommunications, manufacturing, field-service and lab applications. The 108-pg book divides into eight sections, covering a line of wire-wrapping tools, testing and troubleshooting instruments, wire and cable, and assembly products and how to use them. It also features a line of low-cost tools and products for educational and home use. **OK Machine and Tool Corp,** 3455 Conner St, Bronx, NY 10475.

Circle No 385

Setting up a communications network

The 8-pg *Integrated Communications* presents an overview of a product family used to develop a communications network, focusing on unit capabilities as well as their role in such design considerations as reconfiguration flexibility and protocol compatibility. One in a series of four brochures featuring modems, networking products and network-switching and -management products, the booklet explains the principles of multiplexing, switching and automated network control and traces a network's evolution from simple point-to-point applications to multinode and multitiered environments. Diagrams depict a network's growth and increasing complexity. **Codex Corp,** 20 Cabot Blvd, Mansfield, MA 02048.

Circle No 386

Computer graphics: a business tool

All About Business Graphics summarizes the history of computer graphics through CAD/CAM, currently the largest segment of that industry. It focuses on the use of computer graphics as a management tool and discusses business advantages, types of systems available and steps to follow to implement a business-graphics system. A chart lists basic characteristics of 30 systems from 24 vendors. Reported are the results of a user-experience survey, which divides responses into three categories: stand-alone systems, systems that operate on-line to a host computer and time-sharing services. $19. **Datapro Research Corp,** 1805 Underwood Blvd, Delran, NJ 08075.

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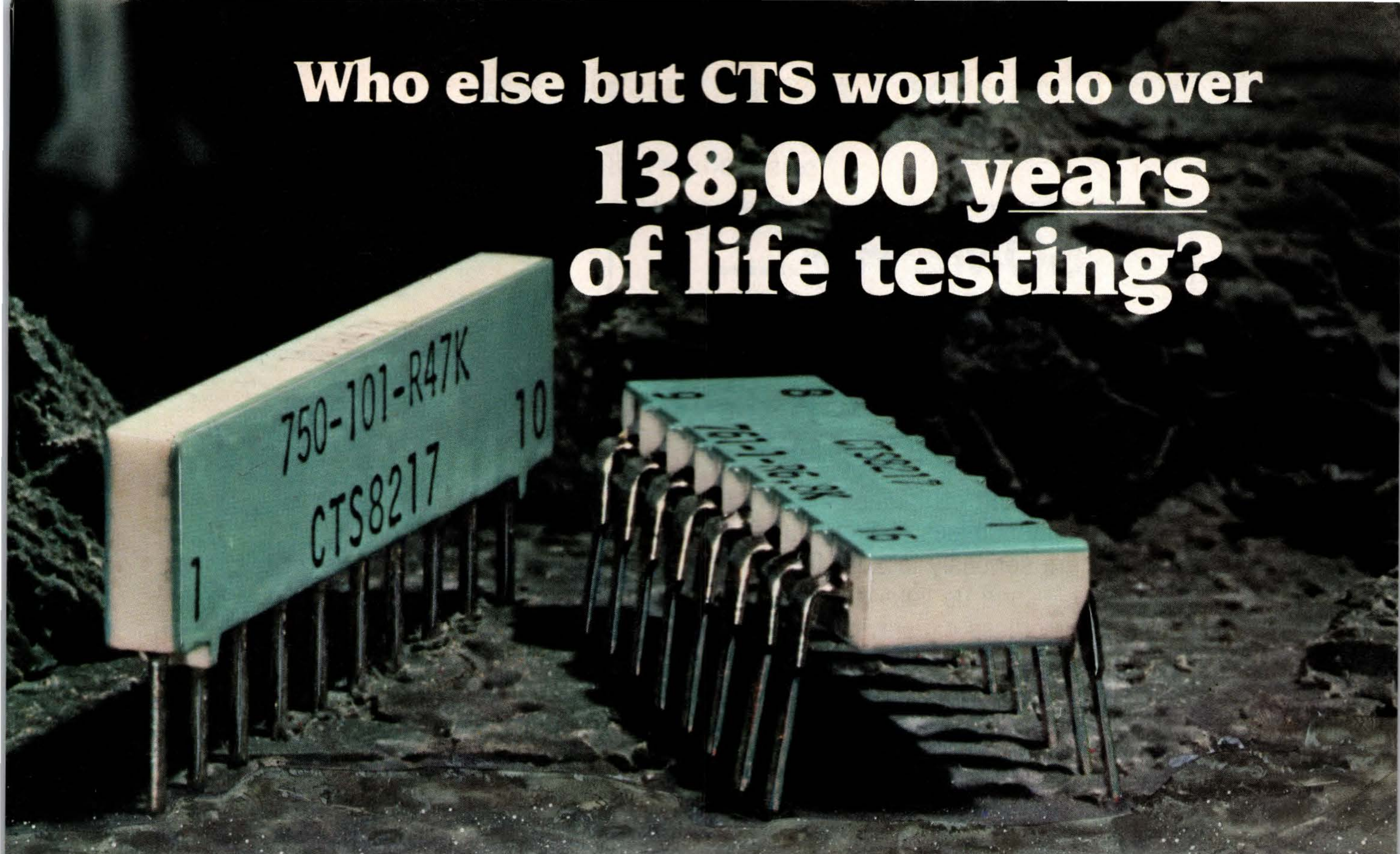

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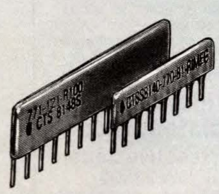

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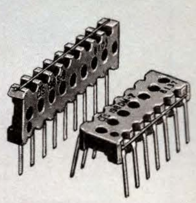

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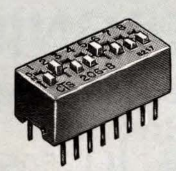

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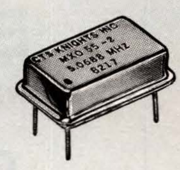

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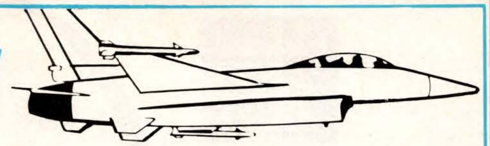

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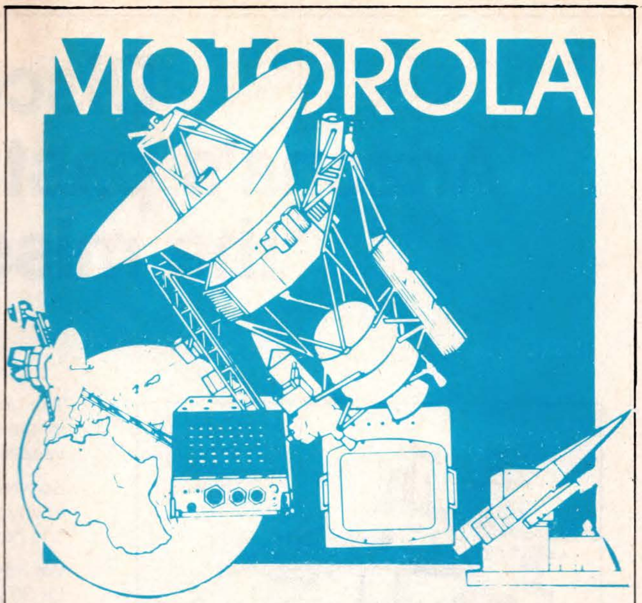

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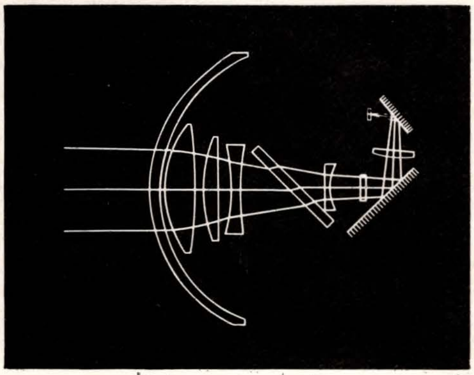

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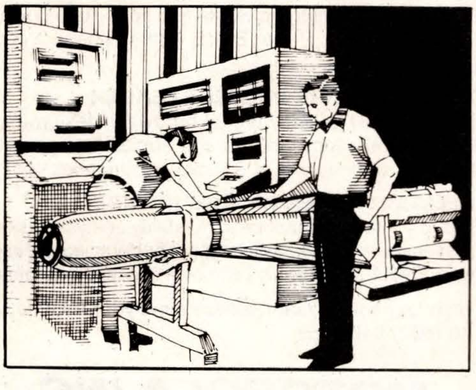

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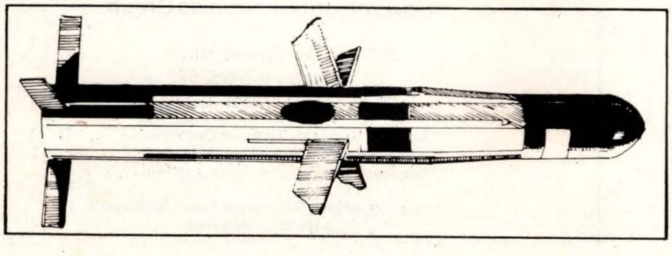

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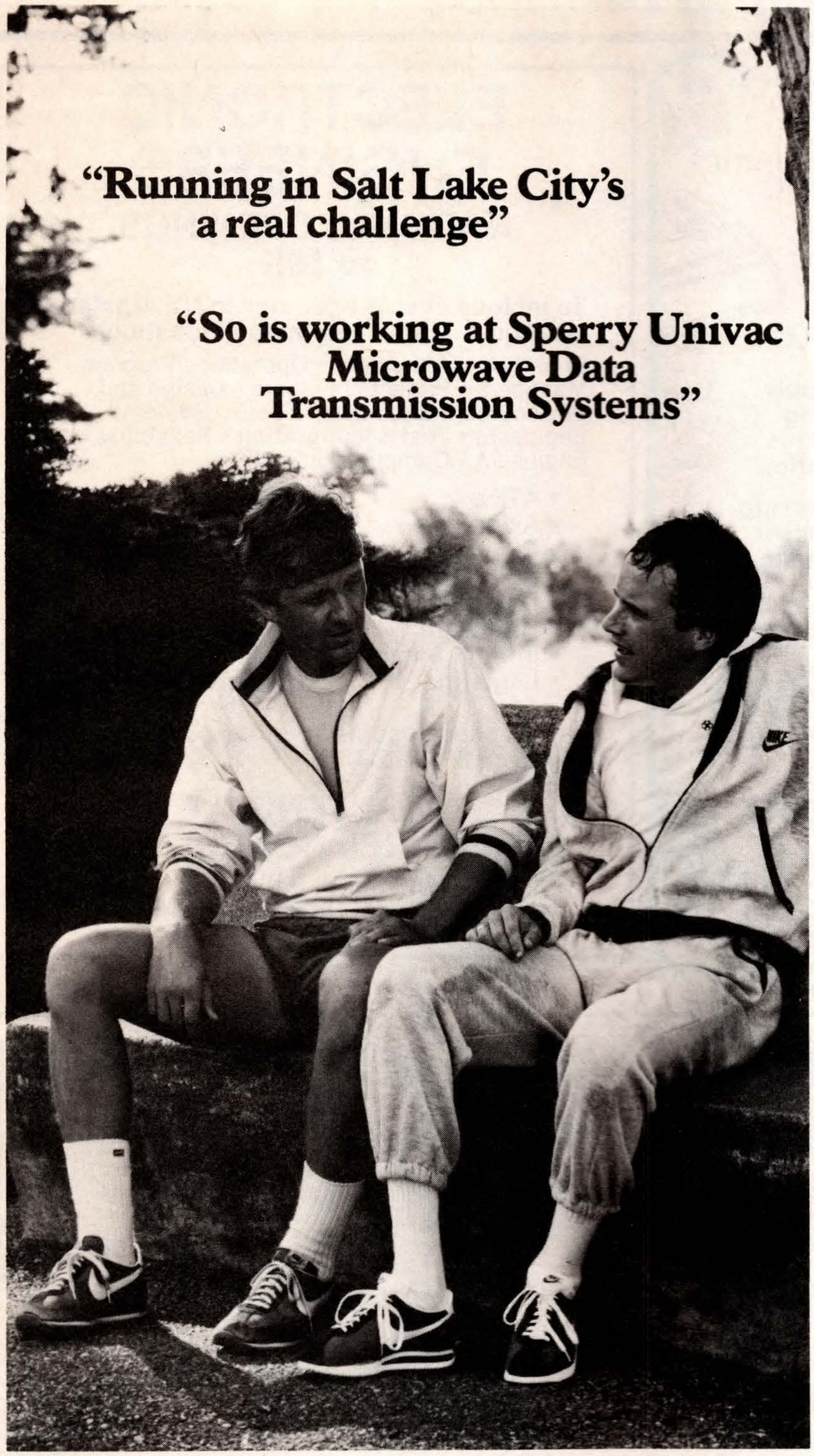
Circle No. 5006 (on page 293 of **EDN**)



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School ________ Location ________ Year Graudated ________ Degree Major ________

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Looking Ahead: Trends and Forecasts

Multilayer-board sales to reach $1.98B in '86

Although most projections see the pc-board market as essentially stagnant, showing little or no real growth until the recession ends, multilayer-pc-board sales, spurred by strong computer, military and telecomm demand, will reach $1.980 billion by 1986, up from 1981's $809 million level, forecasts Gnostic Concepts Inc, Menlo Park, CA. Furthermore, these boards (with four or more layers) will capture an increasing share of total US production of both captive and independently produced boards, Gnostic predicts.

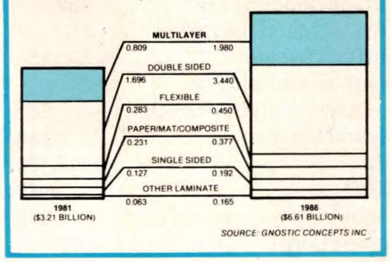
The fastest growing market segment—boards with 10 or more layers—will increase 22.2%/yr, propelled by the growing penetration of these products into nonmainframe-computer, telecomm, instrument and military uses. However, the boards' traditional application area, in mainframe computers, will exhibit only 10% annual market growth, predicts Harvey Miller, president of Kirk Miller Associates (Palo Alto, CA).

Meanwhile, the market for the 4- to 6-layer boards used in minicomputer, backplane and memory applications will see 19%/yr growth, adjusted for inflation.

In related developments:

- Mass-lamination techniques, which join boards with four or more levels together without the use of pins, are providing easy entry into the multilayer market for small firms making single- or double-sided pc boards. Production of mass-laminated boards will thus show healthy growth, rising 18.8%/yr to $1.2 billion in 1986,

US PC-BOARD PRODUCTION ($ BILLION)



Gnostic Concepts predicts, and will account for 60% of all multilayer-board production, estimates BPA Technology and Management Ltd, Surrey, UK.

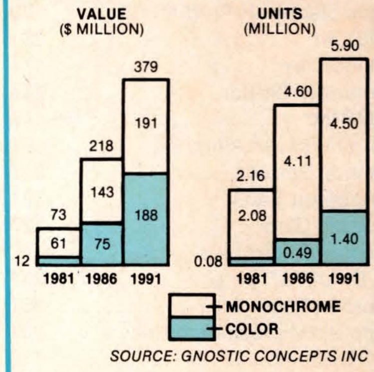
- Polyimide-glass fabric, once restricted primarily to military applications, is finding increasing favor as an alternative to conventional epoxy-impregnated-glass pc-board material. Providing better temperature resistance—to more than 200°C in some versions—and a smaller coefficient of expansion, rigid and flexible polyimide boards will capture $5 million and $9 million, respectively, of the $400 million and $40 million total US board markets, forecasts William Loeb, consultant.

Rising market share seen for color monitors

Color monitors (EDN, November 10, pg 41) will continue to gain market share at the expense of noncolor units through 1991, prompting some analysts to predict the demise of the conventional monochrome computer monitor. US consumption of computer-oriented color CRTs—color monitors' hardware heart—will thus surge at a 45% annual rate from 1981 to 1986 and grow 20%/yr from 1986 to 1991, forecasts Cindy Trish, analyst at Gnostic Concepts Inc.

In sharp contrast, the total

US CONSUMPTION OF CRTs FOR COMPUTER EQUIPMENT



US CRT market, including monochrome devices, will grow only 25%/yr through 1986 and 12% annually through 1991. Color CRTs, moreover, will account for 76% of all units used and 50% of all dollars spent on CRTs for US-produced computer equipment.

"We see no reason why color monitors won't eventually put monochrome monitors out of business," asserts Kevin J Bowler, Nissei Sangyo America Ltd's (Wellesley Hills, MA) color-monitor product manager. "As more and more sophisticated software is developed, the demand for color business graphics also will fuel demand."

Joseph Campbell, Data Display Dept manager at Panasonic Co, however, sees color monitors capturing only about 20% of the computer data-display market. Color, he says, has a certain snob appeal, but monochrome monitors, at least for office applications, are more cost effective and often provide better definition.

Material for this page developed from *Electronic Business* magazine and other sources by Jesse Victor, Senior Staff Editor, and Joan Morrow, Assistant Editor.

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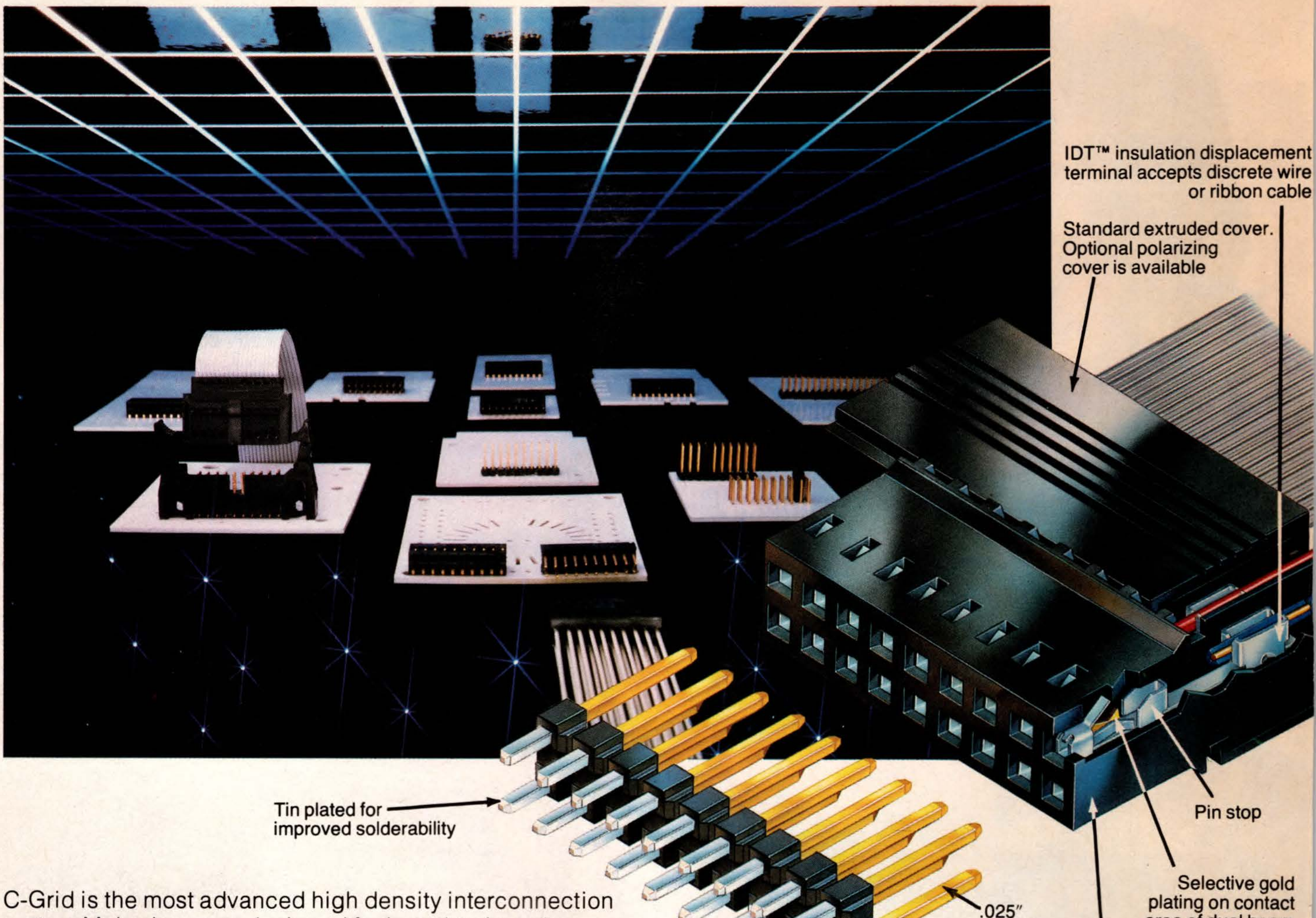

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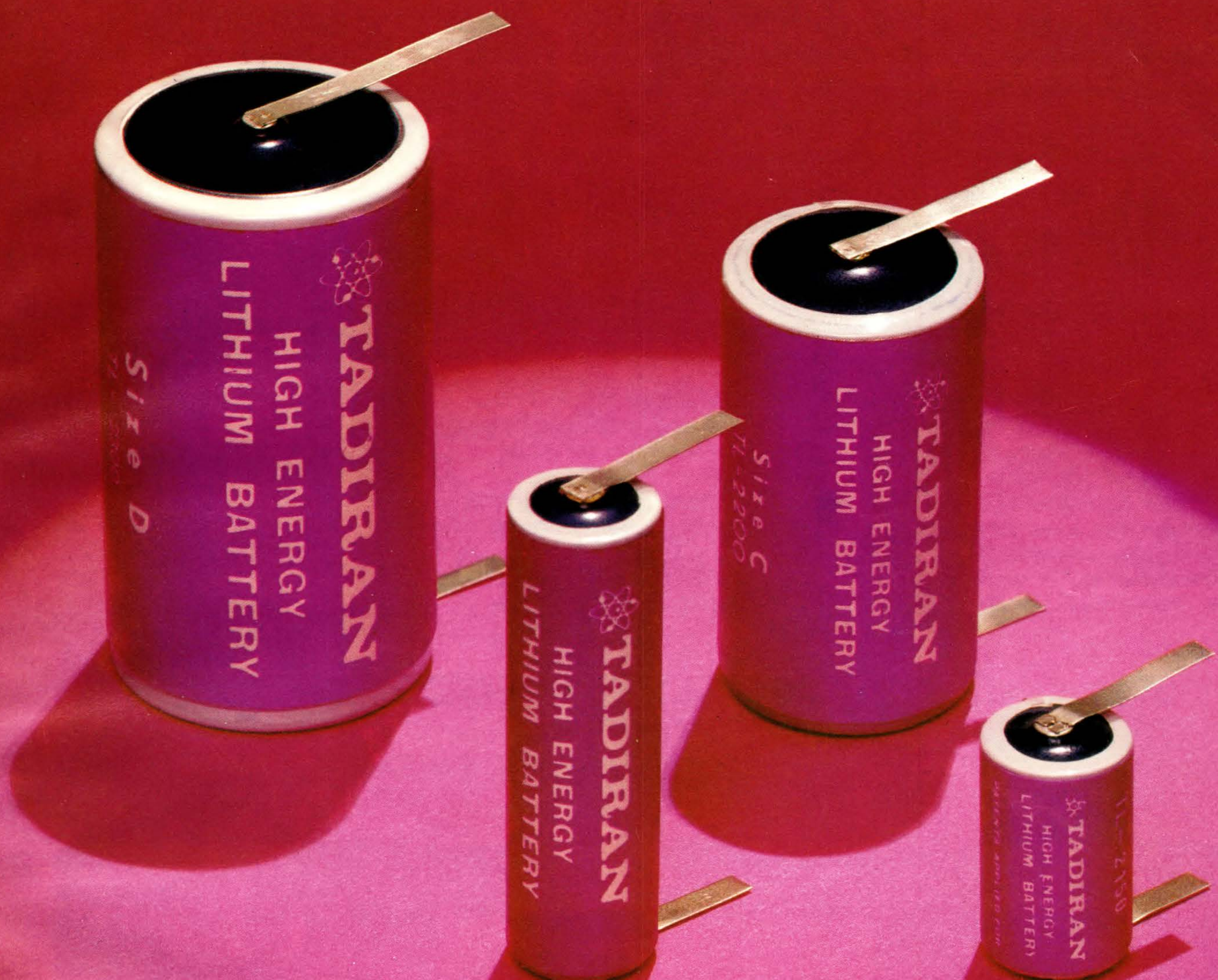

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